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ELECTRONIC DESIGN

7 JUL 1993

APRIL 15, 1993

FOR ENGINEERING AND ENGINEERING MANAGERS--WORLDWIDE

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- ADVANCED TECHNOLOGY SERIES: FLAT-PANEL DISPLAYS
- ELECTRO/93 PREVIEW
- COMPUTER SYSTEMS DESIGN SECTION
- PEASE PORRIDGE

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THE PROBLEM WITH MOST EPLDs IS YOU NEVER KNOW WHAT YOU'LL RUN INTO.

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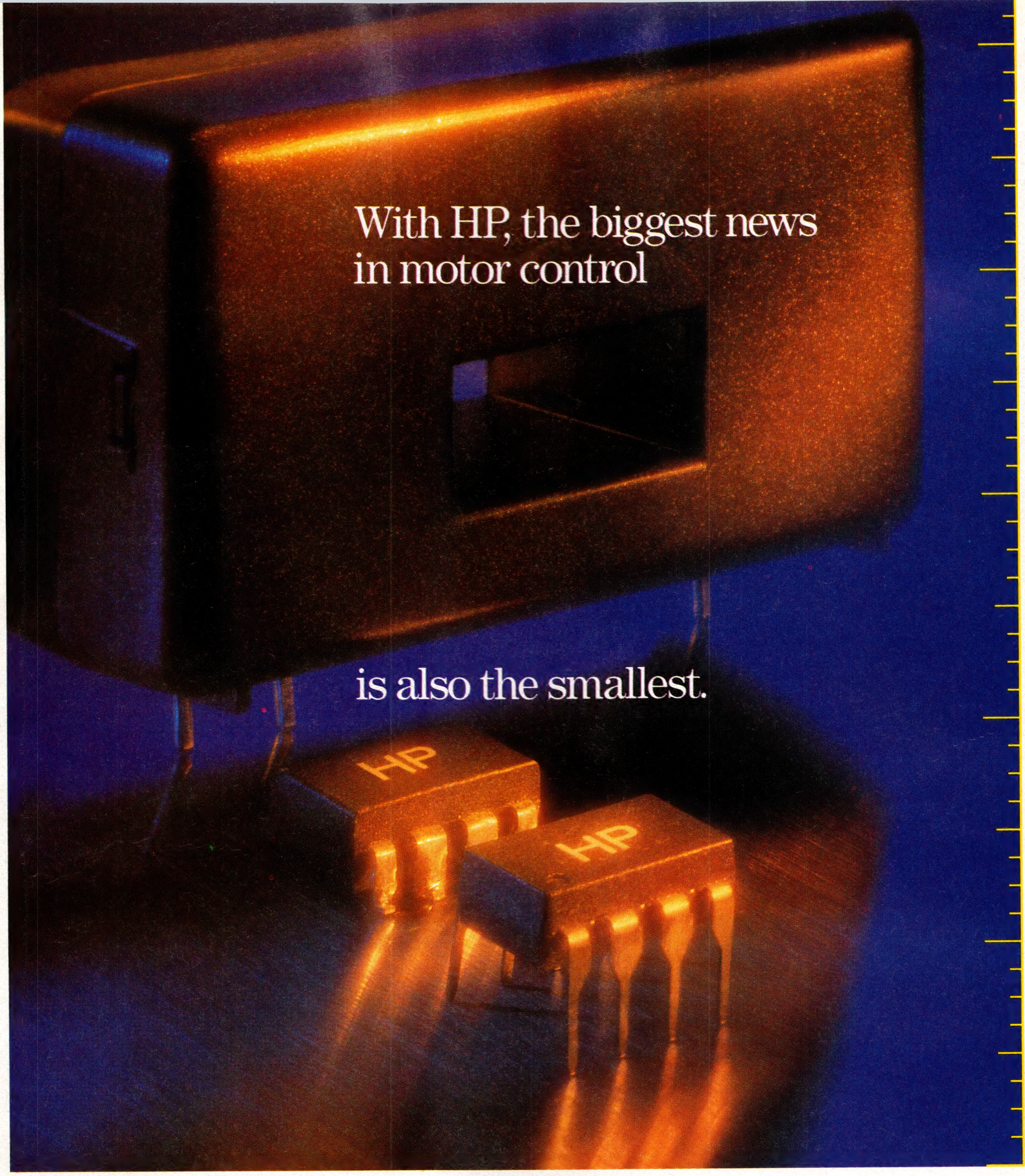

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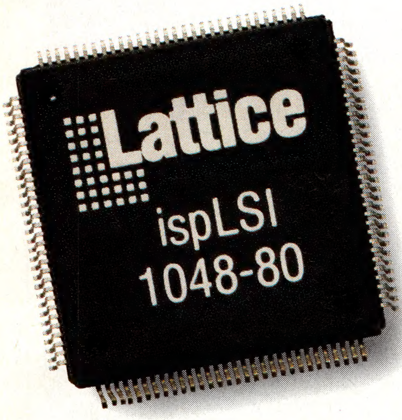

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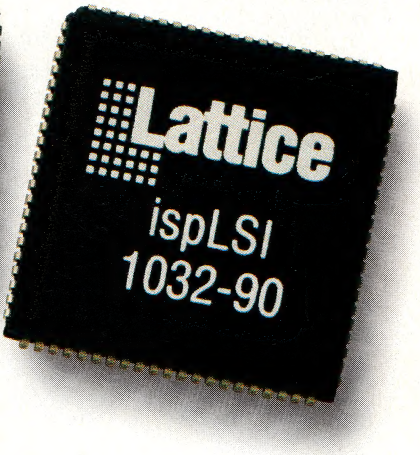

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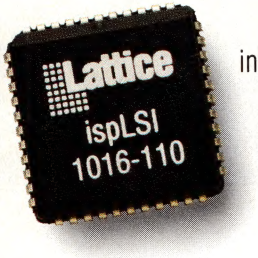

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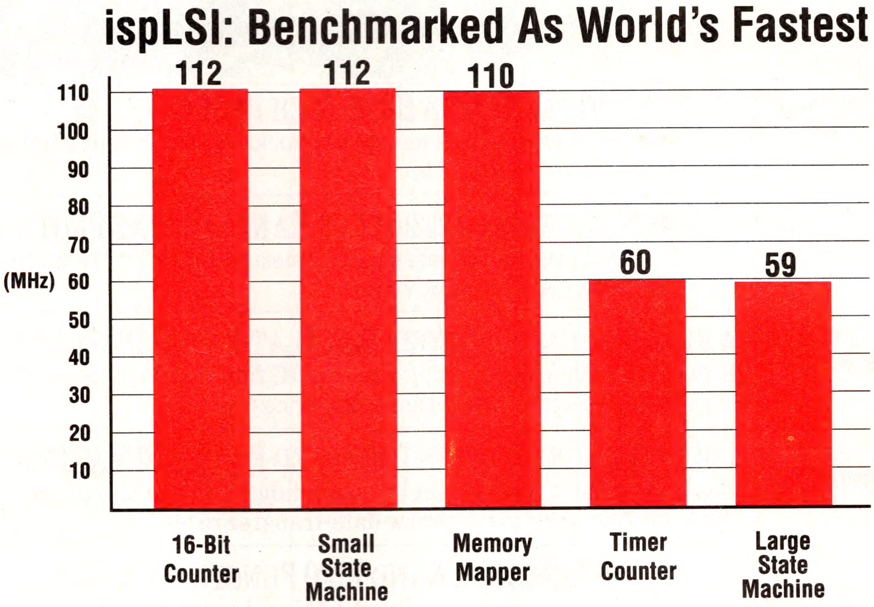

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ELECTRONIC DESIGN 40 YEARS AGO

The following items are reprinted from the Electronic Design issue published 40 years ago this month.

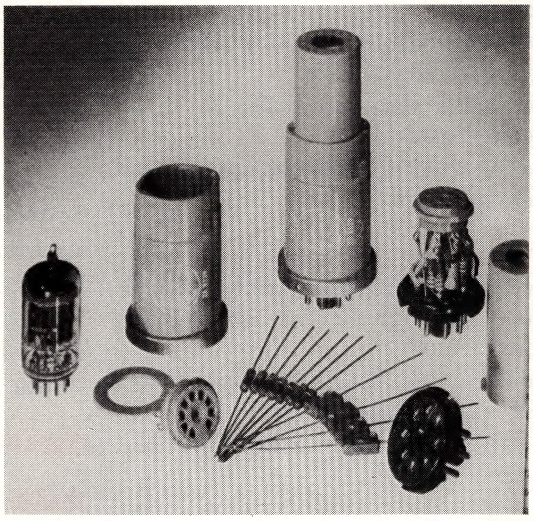
Analog-to-Digit Converter Has Accuracy of 0.1%

The Type 24A "Teleducer" automatically converts analog voltages into decimal digits with an accuracy of 0.1% (1000 counts full scale). It operates upon demand, digitizes an input voltage, and holds the digital representation for a controllable period of time for purposes of display, recording, or any desired readout form. The digital output can be recorded by means of punched cards, an electric typewriter, magnetic tape, or punched tape. Low voltage is digitized without dc-amplification, and high voltage by means of attenuators. The instrument uses a simple-bridge balancing circuit which does not hunt or oscillate and requires only 0.8 sec or less to reach balance. Telecomputing Corp., Burbank, Calif. *(Electronic Design, April 1953, p. 16.)*

A benchtop or rack-mountable unit, this 10-bit converter with its 800-ms conversion time had a front-panel display with three decimal digits: three columns of ten lamps per column.—Ed.

Packaged Plug-In Circuits

Ease of electronic design, reduced service problems, conservation of space, and increased reliability are features provided by this series of packaged plug-in circuits. These characteristics are particularly important and advantageous in equipment where large arrays of similar circuits are banked together, as in computers, data coding telemetering, and similar types of equipment. Originally developed for the Armed Services by the Electronic Engineering Co. of California, these units now are generally available in 26 catalog types and 40 secondary versions. Standard circuits include amplifiers, flip-flops, multivibrators, squaring circuits, pulse gates, crystal oscillators, "and" circuits, "or" circuits, pulse amplifiers, and many others.



These units consist of an octal plug and a miniature tube socket with components mounted turret-style as shown in Fig. 1. The entire unit is encased, including the vacuum tube, in a die-cast aluminum shield assembly 4-1/8" high x 1-1/2" diam. Fig. 1 also shows the R-C components which comprise a typical plug-in flip-flop circuit.

The packaged plug-in circuit presents a series of design advantages. One of the primary features is new freedom for the design engineer, who by using the packaged units as "building blocks" becomes a "block diagram man" in the sense that he may expend his major effort on general equipment configurations and comprehensive circuit considerations. Still other advantages of the plug-in circuit include lower maintenance costs because of the ease of replacement of an entire circuit, thus slashing "down time" on equipment and stepping up the maximum inherent reliability of the equipment itself. Packaged plug-in circuits also reduce the number of individual parts normally stocked, and afford a reduction in the purchasing and material control, as well as many accounting costs. *(Electronic Design, April 1953, p. 12.)*

Here's one flip-flop in about 7 cubic inches. Today, a flip-flop takes up a few cubic micrometers. Nonetheless, this article seems to do a good job of spelling out the advantages of circuit modules, which still are valid.—Ed.

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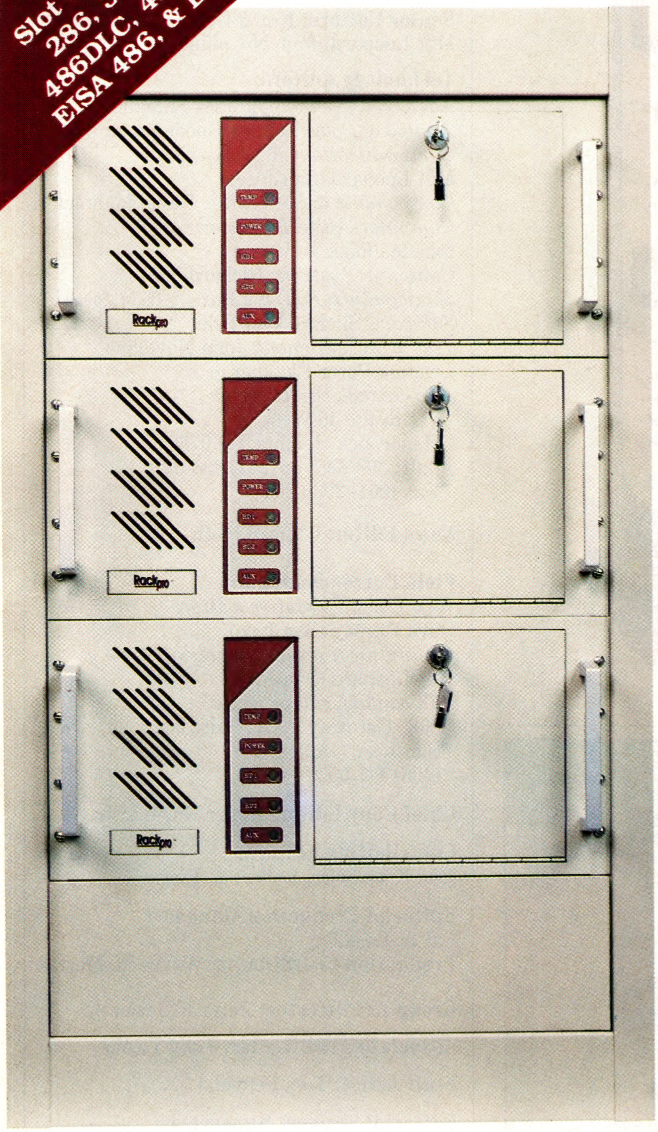

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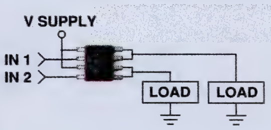

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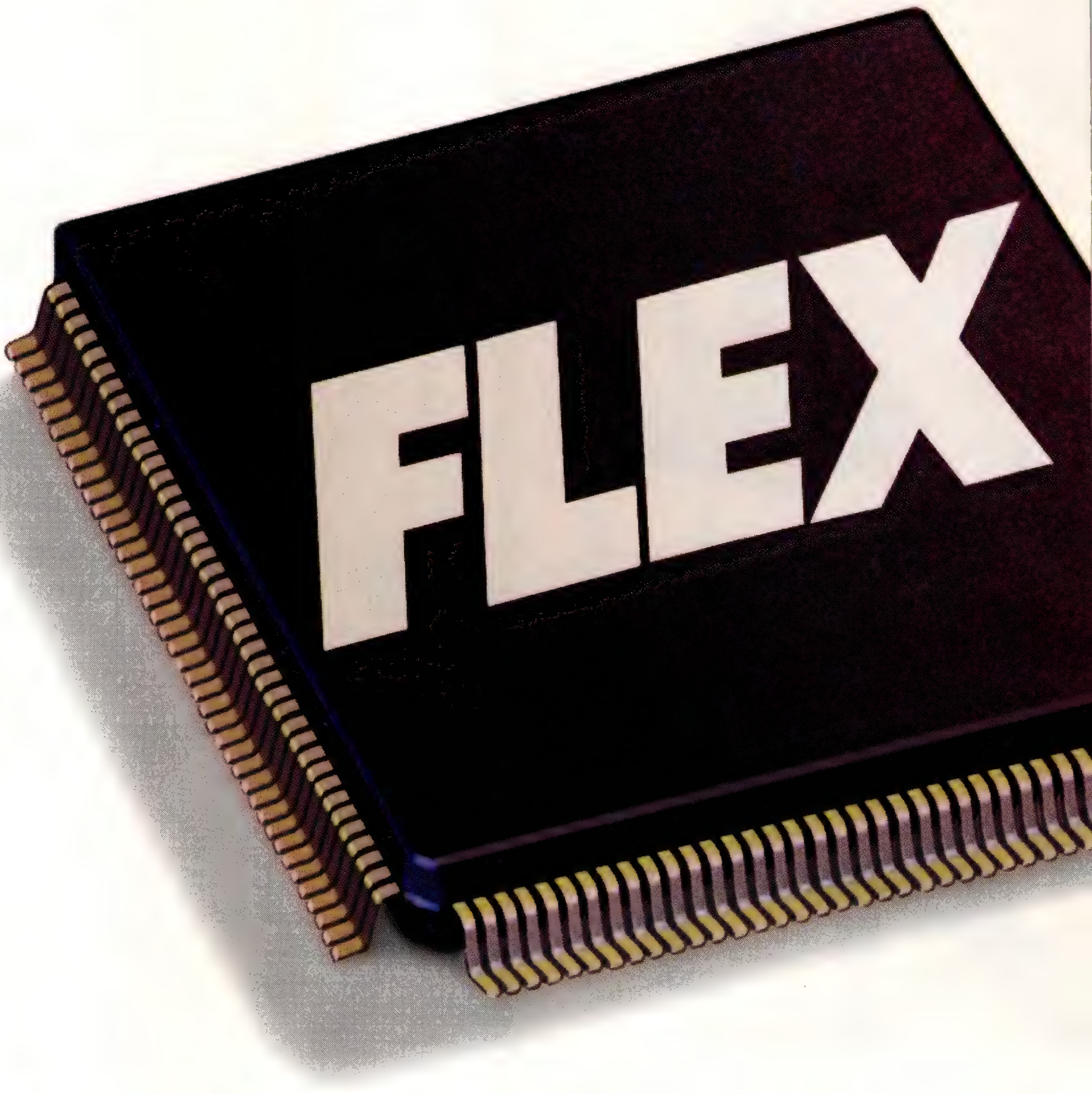

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THE HUMAN SIDE OF ENGINEERING

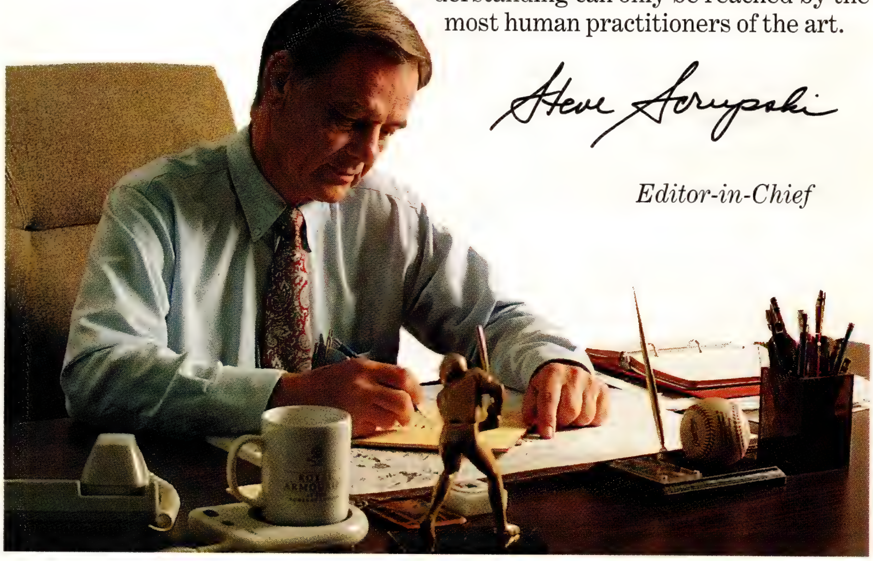
For once, let's put aside the weighty problems of defense industry conversions, engineering employment, and global competition. Besides, it's Income Tax Day, and how much bad news can we take? Instead, let's reflect on the practice of engineering. Engineers are stereotyped as humorless, logical reasoners with little appreciation for the emotional aspects of a problem. But for anyone who is an engineer or knows one, this is far from the truth. Those who read Bob Pease's column regularly in Electronic Design know, for example, how Bob epitomizes the human aspects of engineering. And, although Bob is unique in his own way, most other engineers are just as uniquely humanistic in their own ways.

Engineers, like other professionals, develop a feel for their technology that transcends its scientific and mathematical foundations. I can recall, many years ago, a professor telling us that when we really understood what was happening in a circuit, the operating parameters would cease to be mere numbers, and we would begin to feel the voltage stresses and the currents that were flowing.

It's interesting that the best engineers combine reasoning ability with an intimacy felt toward their designs—a deep understanding of the behavior of the various components—to the point where they begin to personify their designs. In an Idea for Design article now being prepared for publication in a future issue, author W. Stephen Woodward of the University of North Carolina uses a flip-flop's metastability to perform a useful function. In describing the circuit action, he uses an interesting, insightful analogy to describe a flip-flop facing two conflicting signals: "As is common knowledge, it's considered 'mean' to simultaneously assert both Set and Reset because no self-respecting binary device can respond with dignity to a command to be simultaneously on and off."

Another example, from Electronic Design's 40th Anniversary Issue (Nov. 21, 1992) involves Peter Holloway, President of East Coast Labs, Andover, Mass. While discussing his early work, he commented on transistors in the following terms: "Transistors were my pets. A 2N169A was a neurotic poodle—you could make it do neat tricks but it would snap at the slightest overload. The 2N188A was your German shepherd—tough, loyal, but not too swift."

So, as engineers return to the field of battle each day, coping with the threat—or the fact—of a company move or a layoff, or with uncompensated overtime to bring a project in on schedule, or simply with the sinking feeling when they get to the bottom line on their 1040 forms, perhaps it's well to remember that engineering offers lots of opportunity to grow as a person. Sometimes reasoning will only take you so far. Deeper levels of understanding can only be reached by the most human practitioners of the art.



Steve Scrupski

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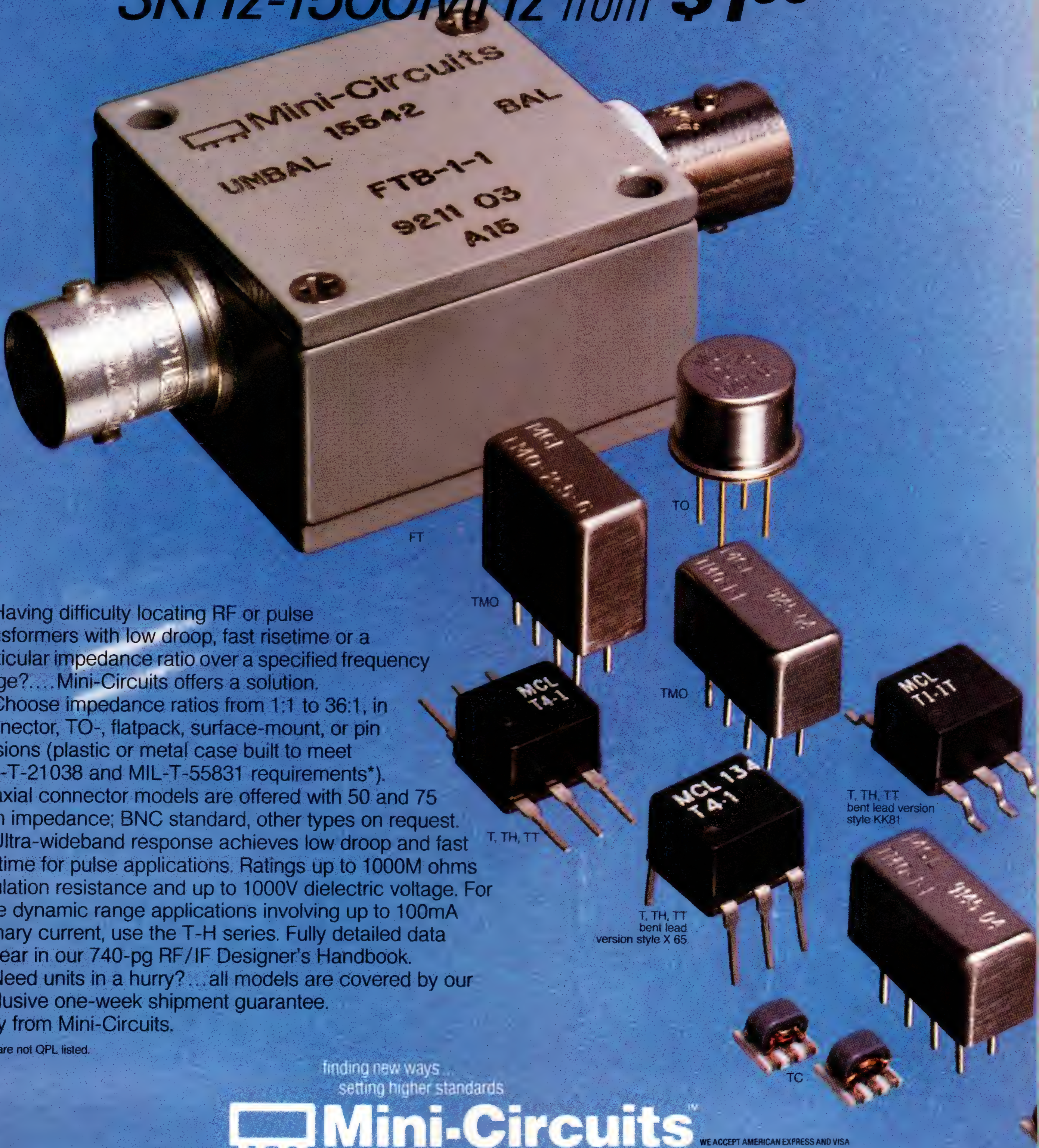

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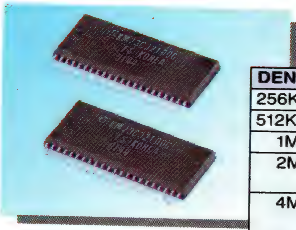
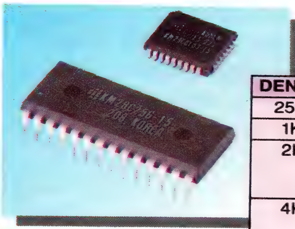


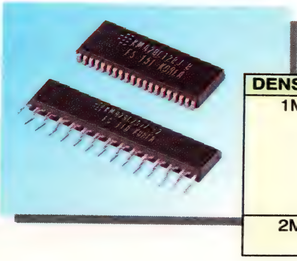
MASK ROM

DENSITY	PART NO.	ORGANIZATION	SPEED (ns)	PACKAGE
256K BIT	KM23C256X	32K X 8	120/150	28DIP/32SOP
512K BIT	KM23C512X	64K X 8	120/150	28DIP/32SOP
1M BIT	KM23C10X0 SERIES	128K X 8	120/150	28DIP/32DIP/32SOP/32PLCC
2M BIT	KM23C2X00 SERIES	256K X 8 128K X 16	100/120	32DIP/32SOP/40DIP/44QFP
4M BIT	KM23C4X00 SERIES	512K X 8 256K X 16	100/120	32DIP/32SOP/32TSOP/40DIP/40SOP/44QFP/44PLCC
8M BIT	KM23C8X00 SERIES	1M X 8 512K X 16	100/120	32DIP/32SOP/32TSOP/42DIP/44SOP/44QFP
16M BIT	KM23C16X00 SERIES	2M X 8 1M X 16	120/150	42DIP/44SOP/64QFP/36DIP
32M BIT	KM23C32X00 SERIES	4M X 8 2M X 16	150/200	42DIP/44SOP/64QFP/36DIP



EEPROM

DENSITY	PART NO.	ORGANIZATION	SPEED	PACKAGE	REMARK
256 BIT	KM93C06/07	16 X 16	1 MHz	8DIP/8SOP	SERIAL
1K BIT	KM93C46/V/I	64 X 16	250 KHz/1 MHz	8DIP/8SOP	
2K BIT	KM93C56/I KM93C57/I	128 X 16 128 X 16 256 X 8	1 MHz 1 MHz 1 MHz	8DIP/8SOP 8DIP/8SOP 8DIP/8SOP	
4K BIT	KM93C66/I KM93C67/I	256 X 16 256 X 16 512 X 8	1 MHz 1 MHz 1 MHz	8DIP/8SOP 8DIP/8SOP 8DIP/8SOP	
16K BIT	KM28C16/J/I KM28C17/J/I	2K X 8 2K X 8	150/200/250 ns 150/200/250 ns	24DIP/32PLCC 28DIP/32PLCC	R/$\overline{B}$
64K BIT	KM28C64A/J/I KM28C65A/J/I	8K X 8 8K X 8	120/150/200 ns 120/150/200 ns	28DIP/32PLCC 28DIP/32PLCC	R/$\overline{B}$
256K BIT	KM28C256/J/I	32K X 8	150/200/250 ns	28DIP/32PLCC	
1M BIT	KM29C010/J/T/I	128K X 8	120/150/200 ns	32DIP/PLCC/TSOP	128B PAGE



VRAM

DENSITY	PART NO.	ORGANIZATION	SPEED (ns)	PACKAGE	PRODUCTION
1M	KM424C256A	RAM 256K X 4 SAM 512 X 4	RAM 60/80/100 SAM 20/20/25	ZIP/SOJ	NOW
	KM424C257	RAM 256K X 4 SAM 512 X 4	RAM 60/80/100 SAM 20/20/25	ZIP/SOJ/TSOP (II)	NOW
	KM428C128	RAM 128K X 8 SAM 256 X 8	RAM 60/80/100 SAM 20/20/25	ZIP/SOJ/TSOP (II)	NOW
2M	KM428C256	RAM 256K X 8 SAM 512 X 8	RAM 60/80/100 SAM 15/20/25	SOJ/TSOP (II)	'92. 12

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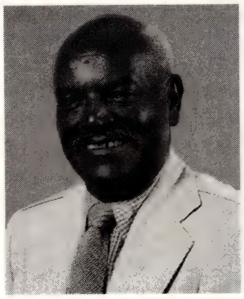


MILT LEONARD
SENIOR EDITOR

Despite modest improvements in on-chip intelligence, sensor technology is still identified as the weakest link in developing most next-generation instrumentation, data-acquisition, and control systems. Sensors in general have been unreliable, rarely offer an accuracy of even 8 bits, sometimes cost more than the controller, and provide few, if any, fault-tolerant or fault-detection capabilities. Nevertheless, industry is responding to increased interest in improved sensor technology for high-volume, low-cost applications. It's intensifying efforts to cram more circuitry on sensor chips by developing "smart sensors."

At this year's Sensors Expo West, held March 2-4 in San Jose, Calif., a set of attributes for the ideal smart sensor was identified by Nader Najafi of MRL/Sensors, Essex Junction, N.H. He said a smart sensor should include all required analog signal-processing functions—amplification, impedance transformation, level translation, filtering, and multiplexing. It should also digitize analog transducer outputs, have an external bidirectional bus for communications, contain a specific address for user access and identification, and be able to execute commands or logical functions received over a digital bus. Other desirable features include compensation of transducer outputs, self-calibration, autoranging, programmability, self-testing or self-diagnostics, fault tolerance, and failure prediction.

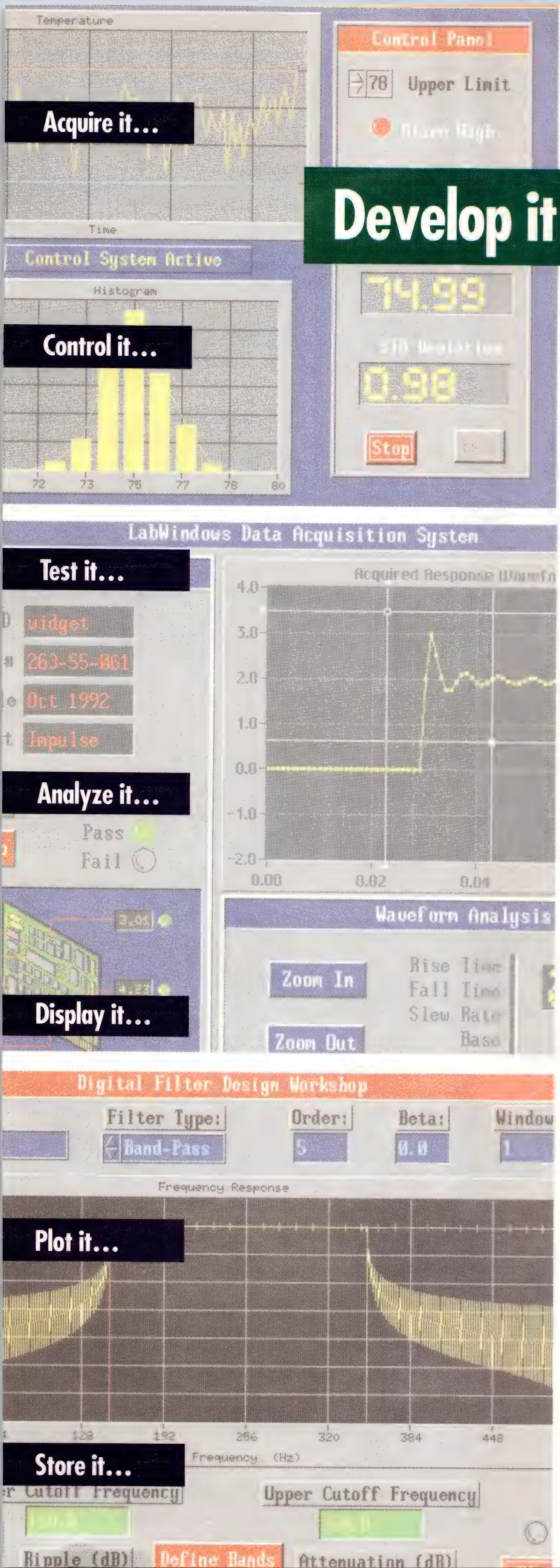
Some of these integrated functions have found their way into hybrid and monolithic sensor designs from leading-edge suppliers. One example is a three-chip hybrid gas analyzer being developed by MRL/Sensors. The module consists of a chip with the sensing element and limited front-end electronics, a signal-processing chip with a microcontroller and a standard communications interface, and a PROM. The company says by merging fabrication processes, the module may soon be integrated into one chip.

The feasibility of manufacturing monolithic smart sensors has already been demonstrated in a few commercially available devices. One example is the "computer-literate" capacitive, all-silicon, low-pressure sensor developed by Monolithic Sensors Inc., Rolling Meadows, Ill. Similar developments are underway at Lucas NovaSensor, Fremont, Calif., and Integrated Sensor Solutions, San Jose, Calif. Although impressive, these developments are still far short of the ideal smart sensor because of several remaining obstacles.

Scientists at IntelliSense Corp., Boston, Mass., and SRI International, Menlo Park, Calif., believe the main obstacle is the incompatibility of conventional fabrication processes with the materials involved. For example, a monolithic pressure sensor that operates in the high-temperature environment would need high-temperature materials in the on-chip signal-processing circuits. A compatible fabrication process that can both define signal-processing circuits and micromachine transducer structures is also required. Still another critical issue is device packaging, which should be considered early in the design phase. The two companies believe it's not unreasonable to envision the package as part of the device fabrication process.

Once these problems are solved, future smart sensors are predicted to have higher levels of integration with analog front ends capable of 14- to 16-bit resolution and linearities better than 1/2 LSB throughout the full analog-signal range. The sensor's integrated signal processor will execute complex signal-conditioning and control algorithms while maintaining a sampling rate high enough to complete analog measurements.

To meet these needs, the sensor design team at Texas Instruments Inc., Dallas, believes the architecture of choice will be the RISC processor because of its ability to maintain high throughput at minimum clock frequency. This reduces noise on the silicon substrate that could interfere with data-conversion circuits.



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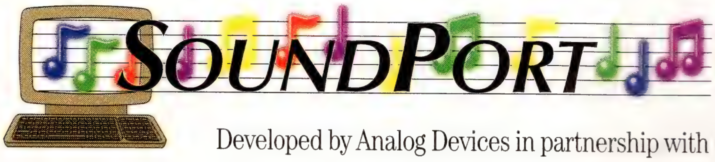

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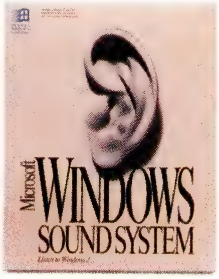

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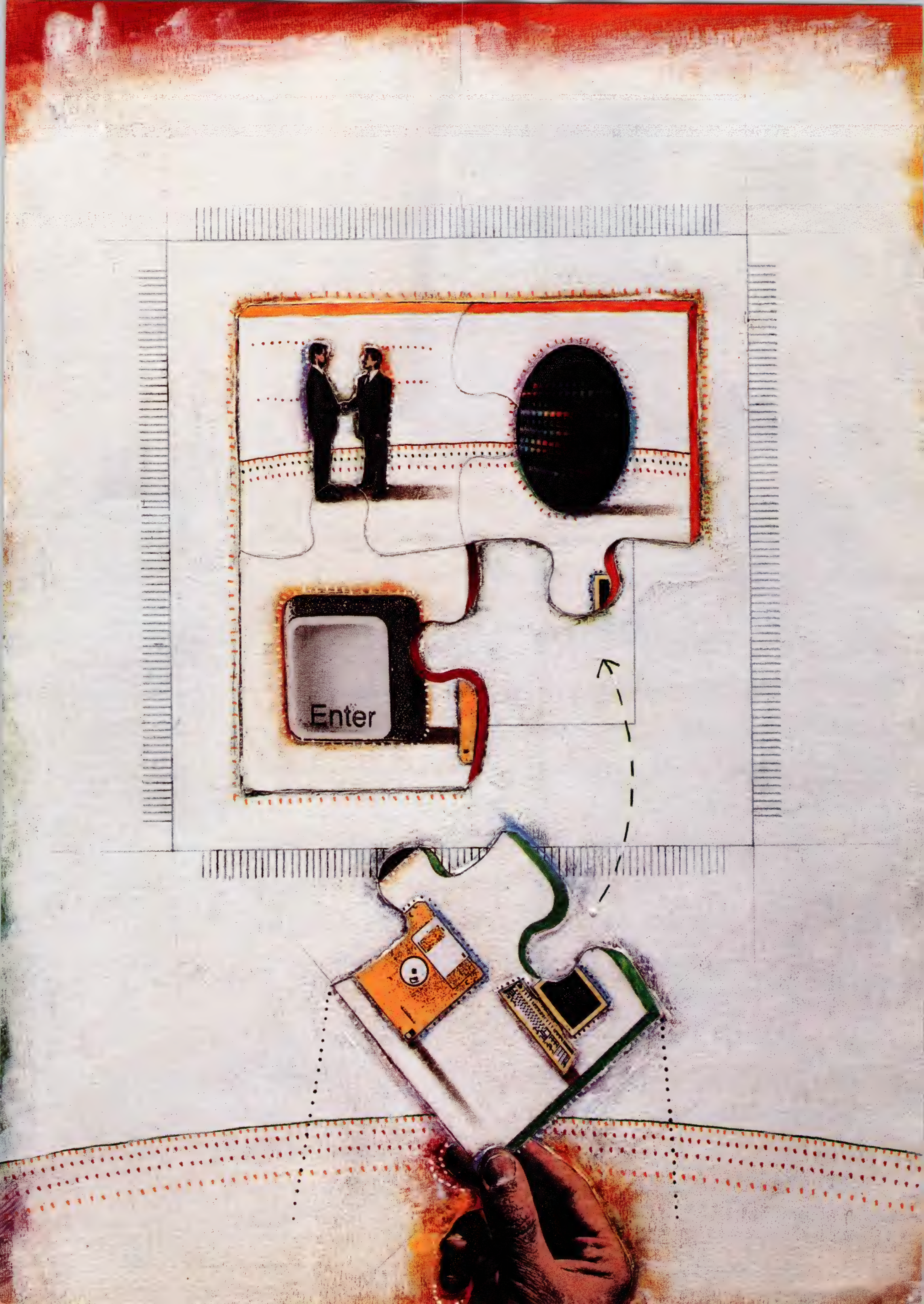
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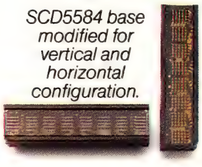

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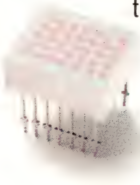

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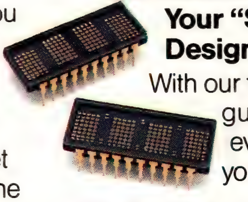

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CIRCLE 191 FOR RESPONSE OUTSIDE THE U.S.

ENERGETIC ATOMS ETCH PHOTORESISTS CLEANLY

Scientists at the Johnson Space Center, Houston, Texas, have used beams of single oxygen atoms with kinetic energies between 1 and 5 eV to anisotropically etch photoresist patterns on silicon wafers. Compared with state-of-the-art methods such as reactive-ion etching, the use of high-energy, neutral-oxygen atoms in the IC lithographic process reduces or eliminates substrate damage because offending high-energy ions and protons are no longer part of the processing. The anisotropic-etching technique is based on the reactivity of oxygen atoms with organic solids, which depends on the kinetic energy of the atoms. A beam of these hyperthermal atoms rapidly attack the photoresist polymer to produce a sharp anisotropic etch. In a fabrication process, the beam would be turned off after etching through the photoresist and before thermalized atoms produced by inelastic collision with the substrate could undercut the pattern. The invention is owned by the National Aeronautics and Space Administration. For information on technology licensing, call (713) 483-3809. *ML*

PCI ADD-IN CARD SPEC IS COMPLETED

The Steering Committee for the Peripheral Component Interconnect (PCI) Special Interest Group has announced the release of the final specifications for PCI local-bus expansion cards. A preliminary specification for add-in cards was distributed last November at Fall Comdex, and input on the final specification was received from system and add-in card manufacturers. The final specification includes all of the necessary information to build a complete system with PCI connectors and add-in cards. This information will be officially released as part of the PCI Release 2.0 specification. The release will also contain support for future devices that operate at lower voltages, such as 3.3 V. Systems containing the PCI connectors should be shipping by the end of the second quarter. For more information, call the Special Interest Group at (503) 696-2000. *RN*

ENHANCED PROCESS TO YIELD ADVANCED PLDS

Through a joint agreement, an advanced 0.65-μm CMOS process developed by Cypress Semiconductor Corp., San Jose, Calif., will let Altera Corp. (also in San Jose) redesign its MAX 5000 (Cypress CY7C34X) series of erasable, programmable-logic devices (EPLDs) for improved speed and lower costs. Process enhancements include smaller geometries and a very thin gate oxide (165 Å) to shrink memory-cell size, cutting overall chip area by about 40%. A smaller area means lower cross-chip propagation delays by close to 50%—down to 15 ns. The reduction in chip area is due in part to structural improvements that make it possible to vertically stack the tungsten-plug contacts and vias that connect the first two layers of metal to the underlying layers. In most other processes, the contacts aren't stacked, thus requiring additional lateral area. The advanced process, which will be used to produce the forthcoming 5000A (7C34XB) family, is also compatible with Cypress' flash memory technology. In addition, Cypress will implement the process in its future high-performance flash-based EPLDs. Samples of the improved MAX chips will be ready in the second half of this year. Contact Cypress at (408) 943-2600 and Altera at (408) 984-2800. *DB*

TRADE ASSOCIATION ORGANIZED FOR PROFIBUS

Widespread use of the Process Fieldbus (Profibus) has pushed a group of companies to join forces and form the Profibus Trade Organization (PTO) in the U. S. Profibus is a high-performance digital field bus standard used for factory automation and process control, primarily in Europe. The open standard (DIN 19245) offers several low-cost off-the-shelf silicon implementations from such companies as Intel, Motorola, NEC, and Siemens, and a number of board- and system-level solutions from PEP Modular Systems and Siemens, among others. A sister organization of the PTO, the European-based Profibus Nutzer Organisation (PNO), will supply part of the capital to fund the PTO. The PTO will pursue the North American adoption of the Profibus standard. The architecture is based on the International Standards Organization's Open Systems Interconnect (ISO OSI) reference model (ISO 7498). For more information, contact Michael Bryant, PTO's executive director at (800) 228-1737. *RN*

ALLIANCE TARGETS SMART SILICON SENSORS

Analog and mixed-signal circuits may soon be combined on the same chip with micromachined sensor structures to create smart silicon sensors. This development stems from an alliance and foundry agreement between Exar Corp., San Jose, Calif., and Silicon Microstructures Inc., Fremont, Calif. Exar makes analog and mixed-signal ICs for use in telecommunications, data communications, microperipherals, and consumer-electronic products. Silicon Microstructures specializes in micromachined standard and custom silicon pressure sensors, accelerometers, and other electromechanical micro-

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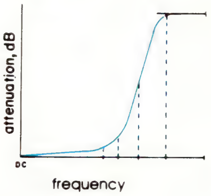
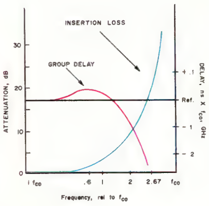
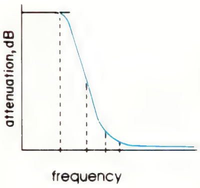
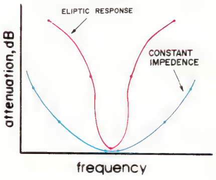




HIGH PASS



BANDPASS



low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-5	DC-5	8-10	10-200
★LP-10.7	DC-11	19-24	24-200
★LP-21.4	DC-22	32-41	41-200
★LP-30	DC-32	47-61	61-200
★LP-50	DC-48	70-90	90-200
★LP-70	DC-60	90-117	117-300
★P-90	DC-81	121-137	167-400
★LP-100	DC-98	146-189	189-400
★LP-150	DC-140	210-300	300-600
★LP-200	DC-190	290-390	390-800
★LP-250	DC-225	320-400	400-1200
★LP-300	DC-270	410-550	550-1200
★LP-450	DC-400	580-750	750-1800
★LP-550	DC-520	750-920	920-2000
★LP-600	DC-680	840-1120	1120-2000
★LP-750	DC-700	1000-1300	1300-2000
★LP-800	DC-720	1080-1400	1400-2000
★LP-850	DC-760	1100-1400	1400-2000
★LP-1000	DC-900	1340-1750	1750-2000
★LP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600
SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2fco X̄	Group Delay Variations, ns Freq. Range, DC thru 2.67fco X̄
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-25	DC-13	13-19	27.5-200	1.8:1
★HP-50	DC-20	20-26	41-200	1.5:1
★HP-100	DC-40	40-55	90-400	1.8:1
★HP-150	DC-70	70-95	133-600	1.8:1
★HP-175	DC-70	70-105	160-800	1.5:1
★HP-200	DC-90	90-116	185-800	1.6:1
★HP-250	DC-100	100-150	225-1200	1.3:1
★HP-300	DC-145	145-170	290-1200	1.7:1
★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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F132 1-2 REVC

structures. Under the agreement, SMI will design its sensors and microstructures to be fabricated by the standard processes used by Exar to manufacture analog circuits. Exar will process the wafers as part of its standard high-volume production runs, and deliver them to SMI for probing, dicing, and packaging. Initial products will include silicon pressure sensors and accelerometers. However, the companies expect to open new product areas by eventually merging their respective expertise in mechanical-structure technologies and circuit design. *ML*

CENTER ESTABLISHED FOR ADVANCED MFG. DATA

A major resource for integrating federal and commercial research and developing advanced-information components has been established at the Sandia National Laboratories, Albuquerque, N.M. The National Center for Advanced Information Components Manufacturing (NCAICM) will help the U. S. Government develop dual-use capabilities for defense and civilian sectors of the economy. NCAICM, which will be operated as a partnership between the Defense Advanced Research Projects Agency (DARPA) and the U. S. Department of Energy (DOE), will complement other U. S. Department of Defense (DOD) microelectronics, optoelectronics, and small-area LCD-based display programs. Research will concentrate on agile manufacturing and packaging technologies associated with advanced silicon ICs, high-speed optoelectronic communications, and electronic systems and subsystems. Two other DOE Defense Program laboratories—Los Alamos National Laboratories in New Mexico and the Lawrence Livermore National Laboratory in California—will support the NCAICM, along with representatives from industry and academia. For more information, contact Bill Alzheimer at Sandia at (505) 844-8035, or Paul Peercy at (505) 845-8927. *RA*

CELLULAR DATA SPEC NEARS COMPLETION

A technology specification that will use standard 30-kHz, analog, cellular-radio channels to transmit digital data at 19.2 kbits/s has taken another step toward finalization. The Cellular Digital Packet Data group (CDPD) released version 0.8 of the specification in late March and is soliciting comments from potential equipment and applications developers prior to publishing the complete specification in July. Using proven channel-hopping and packet-switching technologies, CDPD sends data packets across multiple cellular channels during idle times on each channel. Besides combining several familiar technologies to create CDPD, the sponsors' goal is to use only off-the-shelf components for equipment. Subscribers would add only a standalone unit consisting of an antenna and a modem or modem card that plugs into a PC or other processor. Version 0.8 of the specification describes the airlink, or, how subscriber equipment interfaces with cellular-radio frequencies. Version 0.9, scheduled for release this month, will address the network interface. Security features such as encryption and authentication procedures will be included in the specification as will error correction, two-way data transfer, unacknowledged datagrams (from vending machines, for example), zone broadcasting, and multicasting. CDPD is a joint effort of nine leading cellular carriers including Ameritech, Contel, GTE, McCaw, Nynex and US West. For more information, contact project coordinator Tony Solazzo at (714) 545-9400. *JS*

PYROELECTRIC IR SENSOR TO MONITOR ENVIRONMENT

The engineering model for the first satellite-mounted sensor that doesn't require a cooling system has been developed. The Improved Limb Atmospheric Spectrometer (ILAS), designed by the Matsushita Research Institute, Tokyo, Japan, has been forwarded to the Japan Environment Agency (JEA) to observe the earth's ozone layer. The sensor can measure the ozone layer's concentration, as well as amounts of destructive gases present at different atmospheric altitudes. It will eventually be mounted on the Advanced Earth Observing Satellite (ADEOS), to be launched by Japan's National Space Development Agency in Feb. 1996. Made of lead-titanate ceramic, the sensor incorporates a pyroelectric infrared (IR) detector for IR spectroscopy and is said to be smaller and lighter than other similar types. The sensor model has passed environmental tests for vibration, thermal vacuum, and electromagnetic compatibility, and its ability to measure the characteristics of constituent gas absorption has been confirmed. Following JEA's approval, Matsushita will construct a flight model of the sensor, for delivery by June 1994. In operation, ILAS will collect sunlight and perform simultaneous spectroscopy tests on the IR and visible regions of light, making it the first satellite-based sensor with this capability. Aerosols present in the atmosphere can also be measured. During each satellite orbit, ILAS will twice measure the sunlight that passes through the earth's atmosphere. *RA*

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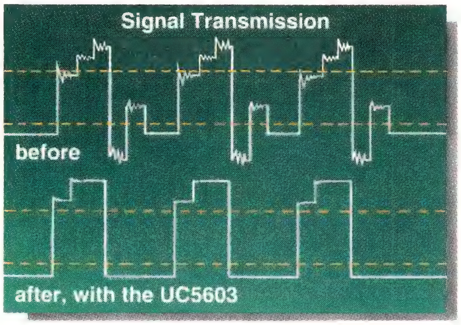

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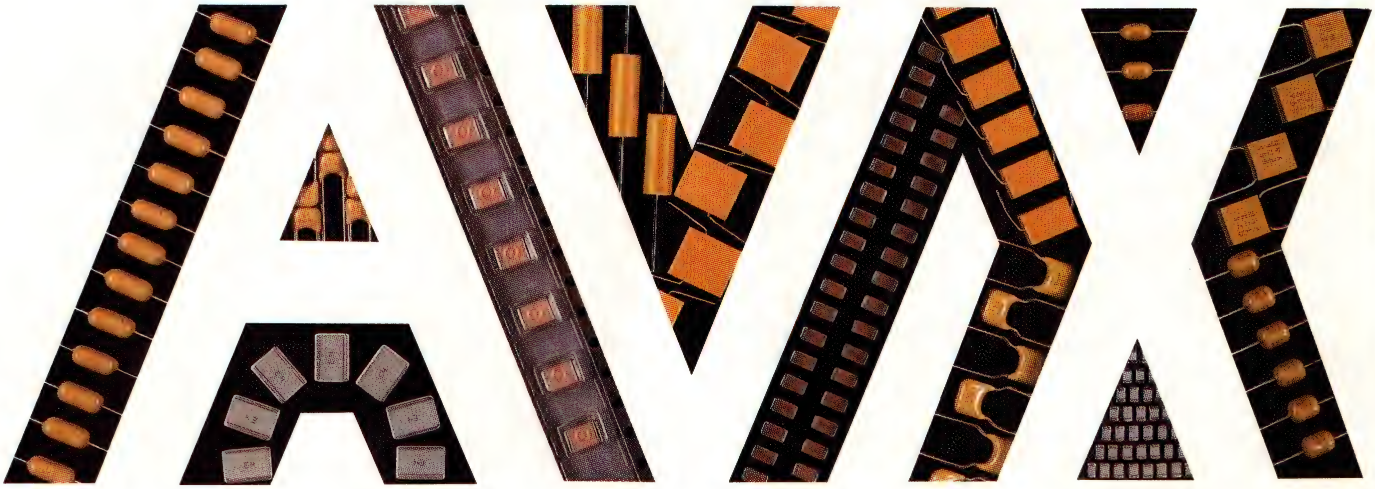

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Dielectrics used: NPO, X7R, Z5U,Y5V					MIL-qualified products available in molded and chip packages					

CIRCLE 242 FOR U.S. RESPONSE CIRCLE 243 FOR RESPONSE OUTSIDE THE U.S.

RESEARCHERS MAKE STRIDES IN DEVELOPING A SINGLE-ELECTRON SEMICONDUCTOR MEMORY

Physicists at the Microelectronics Research Centre at the Cavendish Laboratory, Cambridge, England, working with researchers from Hitachi Europe Ltd., have proved the practicality of making a semiconductor memory structure that uses just one electron to store binary information. The long-term objective is to have memory chips store a terabit—10^{12} bits—of data on a semiconductor die around 2.5 cm^2.

Although that objective could be 15 years from realization, according to Dr. Yutakah Kuwahara, general manager of Hitachi's R&D Centre, promising progress has been made. Researchers have devised a structure that requires some 100 or so electrons for each memory cell, however it's still far from being practical. Based on a gallium-arsenide (GaAs) substrate, it needs to operate at 0.1K, a temperature that's extreme even in the world of cryogenics.

Still, Kuwahara is confident that the structure is the forerunner of real-world mass-memory chips. "Provided we can make physical structures at a 0.5-nm scale, this memory could operate at room temperatures," he says.

In the new memory structure, one bit of information is defined by the exact number of electrons stored at a memory node. This precise definition of the number of electrons is made possible by the Coulomb blockade effect, which causes the movement of individual electrons to be controlled. If an isolated region of conductor is made sufficiently small, the change in stored energy due to the gain or loss of an individual electron results in a larger potential change. Thus, further electrons cannot enter and existing electrons cannot leave.

The principal parts of the single-electron memory cell consist of a multiple-tunnel junction (MTJ) and a gate capacitor *(Fig. 1)*. The memory node is a small conducting region connected to an external circuit via the MTJ and is subject to control by the gate capacitor. Electron transfer to or from the node is possible only through the MTJ, which itself consists of several tunnel junctions in series. The memory-node voltage depends both on the number of electrons at the node and on the voltage applied to the gate.

When the device is within the Coulomb blockade region, electrons cannot enter or exit the memory node *(Fig. 2)*. As the memory-node voltage reaches the boundary of the Coulomb blockade region, one electron enters or leaves and the electron state reverts to the region. After a further discrete increase in the node voltage, the boundary of the Coulomb blockade region is again reached and another electron can be transferred.

To discharge the node, the added electrons must be removed one at a time, requiring a definite voltage change. This leads to hysteresis, with two possible electron states for the same applied voltage, enabling the memory states to be defined. In general, one bit of information can be represented by +N and –N electron number states, where N is determined by the ratio of the gate capacitor's capacitance to that of the MTJ.

To utilize the Coulomb blockade effect, the structures must be shrunk to increase the electron-charging energy. The charging energy is roughly inversely proportional to the linear dimension of the device.

Kuwahara says that to meet this requirement for very small structures, the researchers fabricated a new structure with side-gated channels in delta-doped GaAs material *(Fig. 3)*. The electron channel is a few atomic layers deep, in an otherwise insulating GaAs substrate.

The fine patterns of the side gate and the MTJ are defined by a very-high-resolution electron-beam lithography technique. Kuwahara says that this equipment is only available at Cambridge.

The rate of electron transfer through the MTJ is tunable because applying a negative voltage to the side gate narrows the electron channel in the MTJ. After adjusting the side-gate voltage, it's possible to control the entrance and exit of one electron at a time.

Kuwahara says that, "Although further studies will be necessary for elucidating the mechanism, we believe that dopants inside the MTJ create tunnel barriers at intervals of several tens of nanometers."

The same fabrication process was used to implement a Coulomb blockade electrometer. Such an electrometer can detect the voltage on the memory node with minimum interference to the electrons on the node.

"At zero gate voltage, two states are seen. These two states correspond to the excess or shortfall of a discrete number of electrons. In this experimental memory structure, this is designed to be 100 electrons," Kuwahara says. "It is possible to reduce the number of electrons and represent a binary code bit with a single electron, for

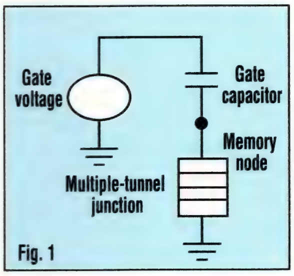

Fig. 1

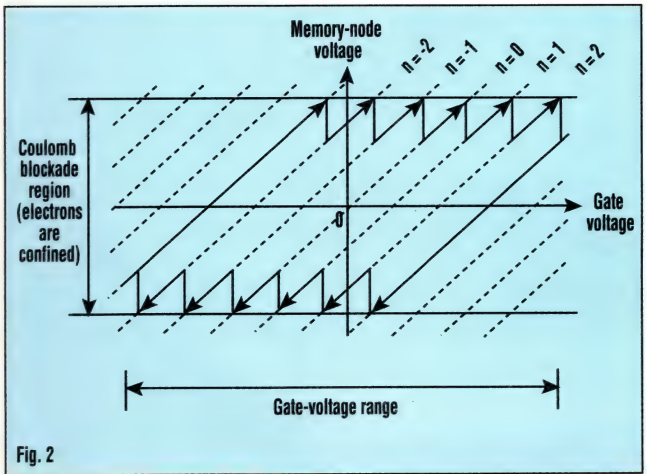

Fig. 2

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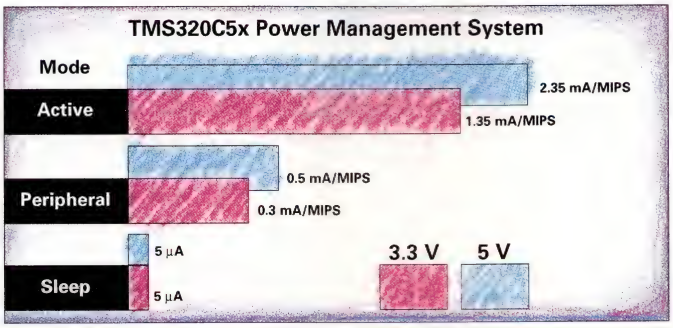

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CIRCLE 258

00-7862B3ae

example, by redesigning the gate capacitor with geometries measured in a few nanometers."

To put the device's potential in perspective, Kuwahara points out that a present state-of-the-art 16-Mbit memory chip contains approximately 50,000 electrons that combined store just one bit of information. "This number is required to ensure immunity from soft errors caused when alpha particles create electron-hole pairs in a semiconductor chip and destroy information," he adds.

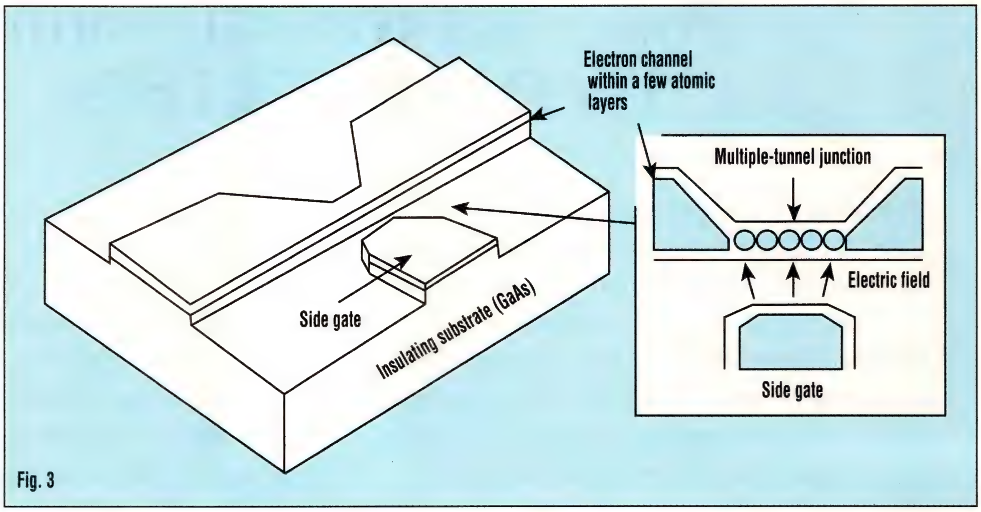
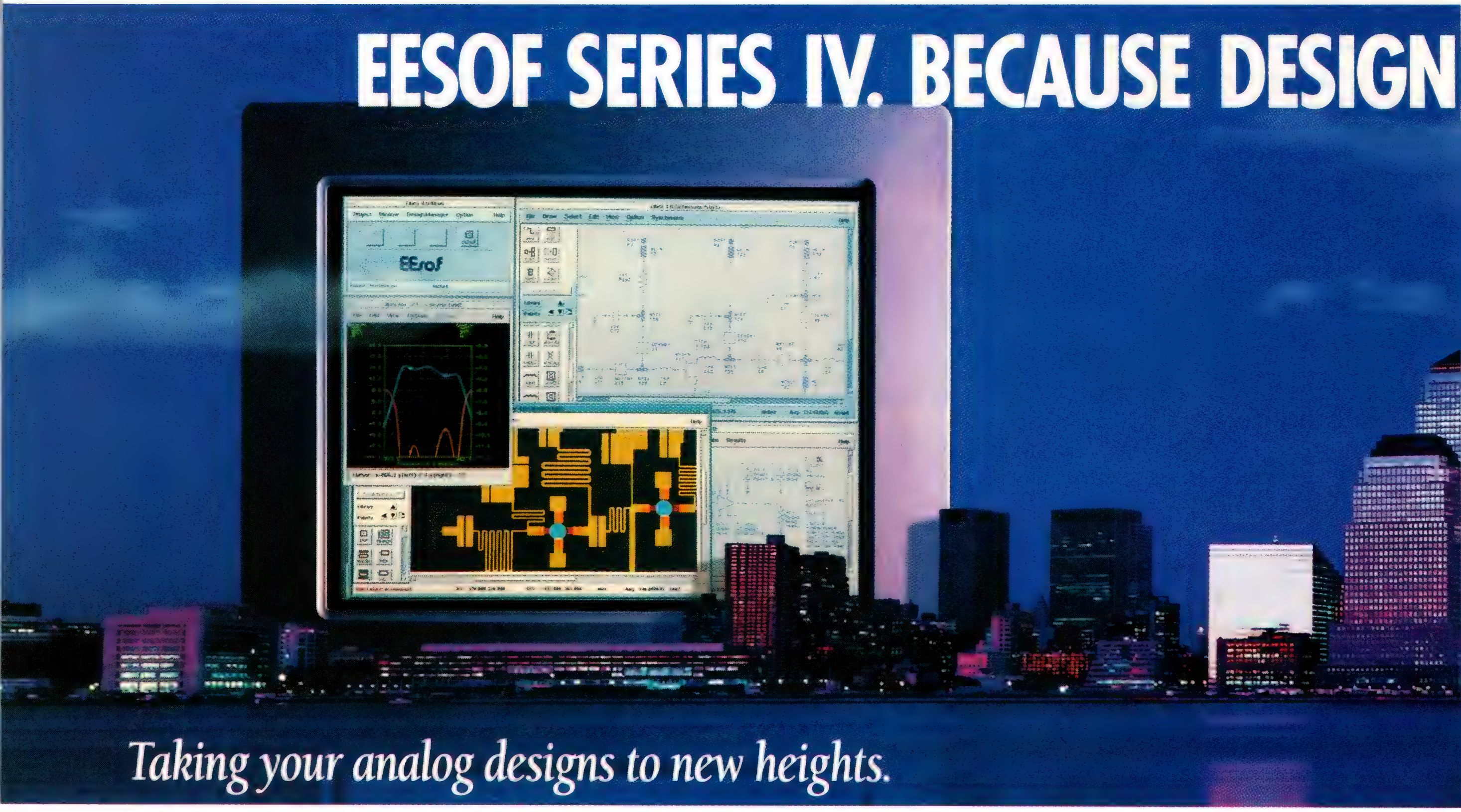


Fig. 3

This problem results from semiconductor devices relying on operating principles based on the average behavior of many electrons. In turn, there's a minimum number required to represent 1 bit of data. "If the number of electrons in a conventional structure is reduced below 1000, fluctuations in electron numbers become relatively large, so we cannot control their number with the required precision," he says.

Kuwahara goes on, "However, if we can gain full control over individual electrons, then we can reduce their number to a very precise quantity and eventually to one." Moreover, the implications for power dissipation are dramatic. He says that a present 16-Mbit memory chip consumes around 0.1 W. "If we were to construct a 1-Tbit memory using a number of 16-Mbit chips, power consumption increases to around 10 kW and that is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clearly impossible for mobile applications."

On the other hand, he asserts that for a room-temperature single-electron memory, a 1-Tbit chip would dissipate less than 0.1 W. At the same time, he feels that a 1-Tbit memory made with 16-Mbit chips would cover 100 square yards of silicon, while just 1 in.^{2} of silicon would be needed for the single electron-cell equivalent.

Success then hinges on the practicality of pico-engineering structures almost at a sub-atomic level. This is where other Hitachi researchers are already making progress. At a 1991 technology exhibition held in London, England, they demonstrated their ability to remove and replace single atoms from the surface of a solid material.

Working at room temperature, the operation involves a scanning-tunnelling microscope (STM), first to view the atomic structure at the surface of the material and then to position a metal probe at a constant 10 Å above the surface. It is lowered to 3 Å over an atom that's to be detached. By applying voltage pluses between probe and surface, individual atoms could be detached. To demonstrate the control they had achieved over the process, the scientists managed to write a message "Peace 91, HTRL" on the surface of a molybdenum sulfide substrate by removing individual sulfur atoms.

For more information, contact Hitachi Europe Ltd., R&D Headquarters, Whitebrook Park, Lower Cookham Rd., Maidenhead, Berkshire, SL6 8YA England; phone: +44 (0)628 585000. Or Hitachi Europe Ltd., Cavendish Laboratory, Madingley Rd., Cambridge, CB3 0HE England; phone: +44 (0)223 467944.

PETER FLETCHER

CERAMIC-SUBSTRATE TECHNOLOGY CREATES REWORKABLE MCMs

Reworkability, a major obstacle to the widespread adoption of multichip-module (MCM) packaging, may have fallen to a ceramic-substrate technology that also promises very high speed and density. The substrates represent another element in the emerging MCM infrastructure that endeavors to propagate the technology throughout the industry and end the so-called packaging bottleneck that stifles high-performance ICs.

The sintered-ceramic substrates employ precision-drilled vias filled with a tungsten-copper composite, so that the thermal-expansion coefficient of the filled vias matches that of the ceramic. When combined with thin-film circuitry, the substrate has multiple application possibilities in microwave amplifier, filter, and oscillator circuits, as well as in single-chip and

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multichip digital circuits. Tests have been conducted at up to 26 GHz for single-chip packages. Such speeds are possible because of the substrate's extremely low parasitics (inductance of 0.2 nH and resistance of less than 2 mΩ).

The Via/Plane substrate, developed by Micro Substrates Corp., Tempe, Ariz., is created on sintered alumina, aluminum nitride, or beryllia. After the vias are drilled as small as 0.005 in., they're filled with tungsten and sintered, leaving a porous mass to be filled in with copper. The material is highly planar and is finely polished.

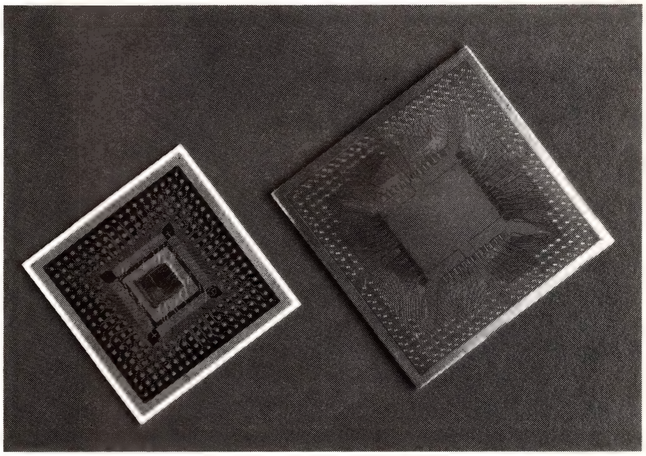
In most applications, devices are mounted directly on the vias themselves. This delivers the lowest possible inductance path to the ground plane mounted on the reverse side. It also provides an effective thermal path, with typical thermal resistance in the vias of 0.5°C/W. High-performance RF and microwave packages can be fabricated by directly attaching the leads onto the vias, thereby eliminating the usual hermetic enclosures with their costly glass-to-metal seals that are prone to failure.

In MCM thin-film (MCM-D) applications, the substrate offers some advantages compared with other materials. For instance, silicon-dioxide substrates are very fragile and require a ceramic or metal carrier, according to Ram Panicker, president of Micro Substrates. Also, only one side of the substrate is available for both circuits and chip mounting. If any of the ICs is bad, attempts at rework typically ruin the circuitry.

With the Via/Plane substrate, both sides of the substrate are available for use. One side can be layered with the thin-film circuitry and connected through the vias to the chips on the other side. Thus, for the first time, rework becomes possible for MCM-D modules.

For digital packaging applications, the Via/Plane substrate can be patterned with multilayer copper-polyimide thin-film circuitry, where it represents an alternative to cofired ceramic technology *(see the photo)*. The fine-pitch chip carriers with 0.001-in. copper traces at a 0.002-in. pitch accept any and all automatic die-bonding techniques. Pins can be brazed directly onto the vias, typically at a 0.05-in. pitch, to reduce the size of very-high-I/O-count PGAs to half that of an equivalent cofired package. Pad-grid arrays can be made at a 0.025-in. pitch.

DAVID MALINIAK



MCM MATERIALS GAINS HAVE DIAMOND'S GLITTER

Many of the benefits derived from multichip-module (MCM) packaging depend upon the materials used in those packages. The physical properties of the substrates, in particular, determine the modules' speed and power handling limitations.

In the search for materials that enable MCMs to bear the wattage of forthcoming generations of ICs, researchers are turning to synthetic diamond as a substrate material because of its extremely high thermal conductivity *(see the table)*. In fact, diamond has the highest thermal conductivity of any known solid material—about five times higher than that of copper or silver. Some recent developments point to diamond's promise as an MCM substrate, especially as its cost begins to fall with mass production.

So far, some types of circuitry have resisted the miniaturization made possible by MCM technology. Most notably, power circuits, because of their thermal loads, are difficult to implement in MCMs. A team of researchers at Sandia National Labs in Livermore, Calif., and Albuquerque, N.M., however, has applied synthetic diamond substrates to the MCM packaging of the power-electronics subsystem for a flight computer. The application's reliability requirements ruled out the use of active cooling, so the module had to rely on its inherent passive thermal conductivity.

Though the application was demanding (device temperatures could not exceed 150°C when starting from an initial temperature of 110°C), early thermal models of the MCM show that the temperature rise of the circuitry will come in at 35°C, or 5°C under its thermal budget. In contrast, an aluminum-nitride substrate allows the devices to get much hotter.

But the researchers found that the advantage of using diamond as a substrate is lost if care isn't exercised in assembling and packaging the MCM. Particular emphasis must be placed on die mounting and on the mounting and performance of the secondary package for the module.

Burgeoning interest in 3D packaging and its application to MCMs has also caused concern for power-dissipation limits, especially when high-power, high-frequency ICs are involved. Engineers at Norton Diamond Film, Northboro, Mass., Technology Applications, Thousand Oaks, Calif., and E-Systems' Garland Div., Dallas, have joined forces on a project, sponsored by the U. S. Defense Advanced Research Projects Agency (DARPA), that proposes to stack several diamond substrates.

The concept involves a stack of alternating layers of diamond substrates, each with ICs and interconnects attached to or fabricated on the diamond, and a precision plastic spacer layer. Conductive "fuzz buttons" are placed in ar-

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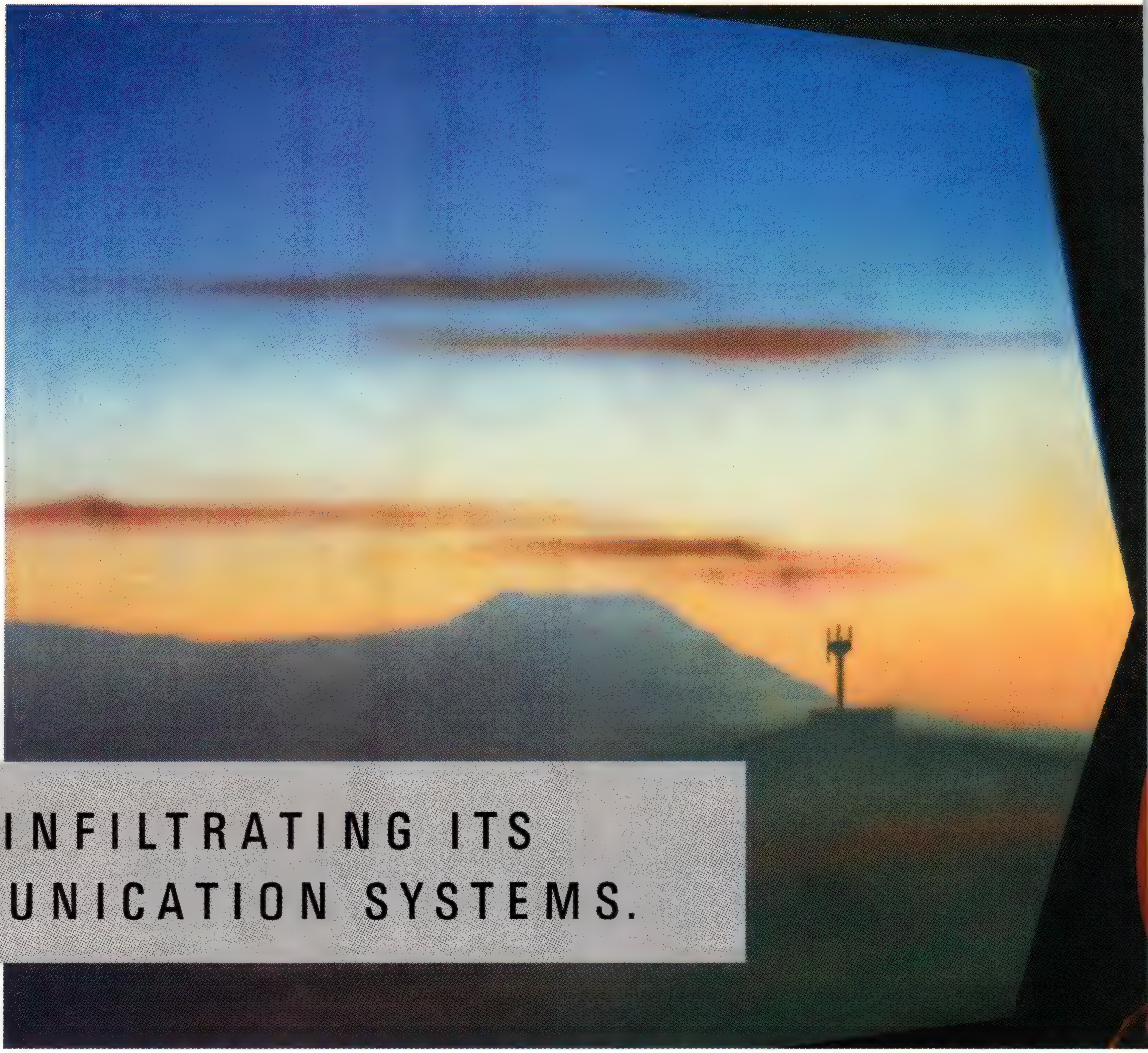

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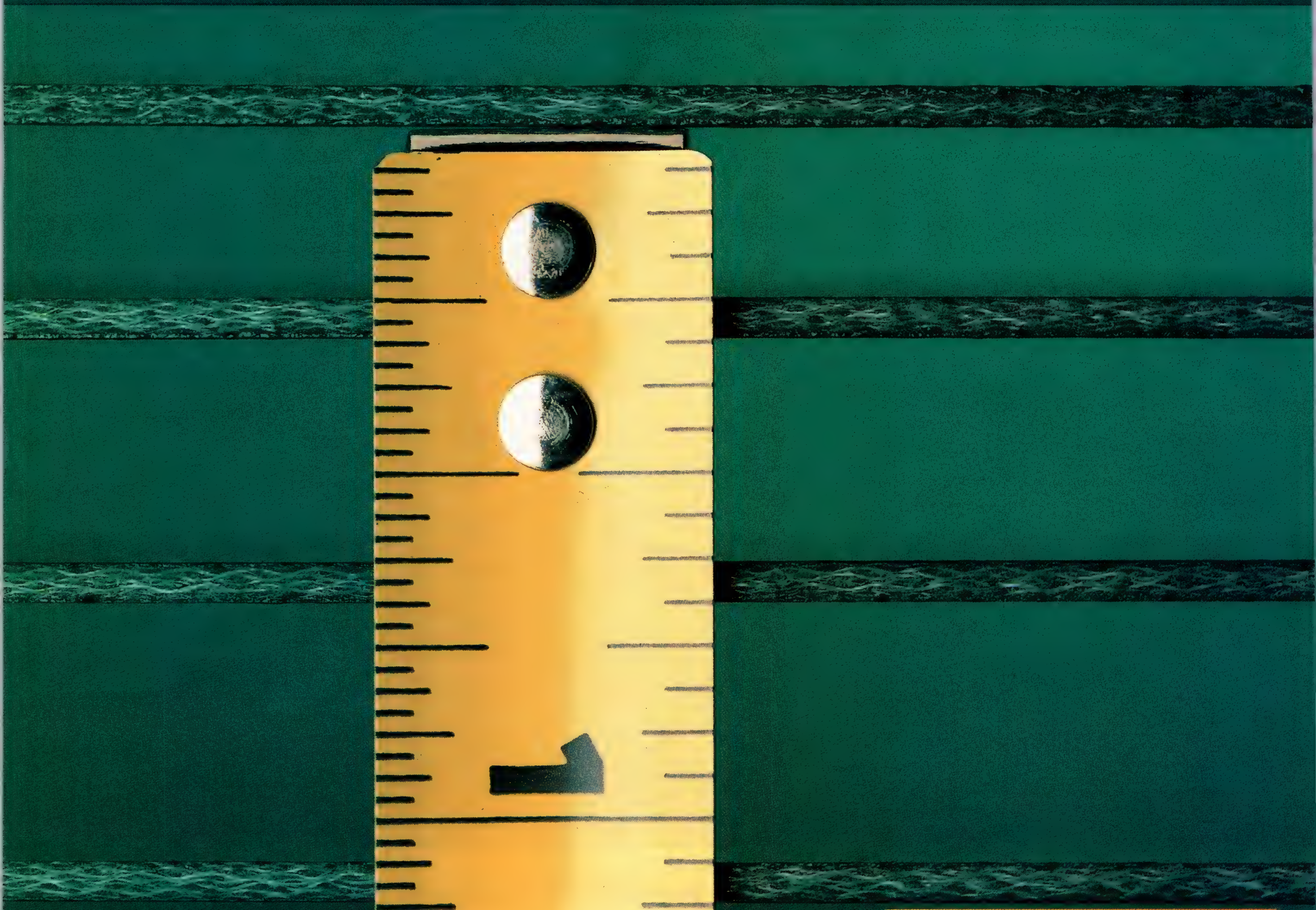

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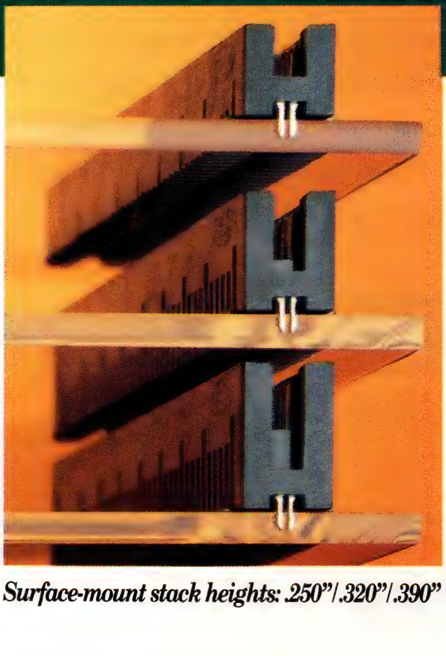

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PROPERTY COMPARISON OF MCM SUBSTRATES

	CVD diamond	Aluminum nitride	Silicon	96% aluminum oxide
Thermal conductivity (W/cm K)	10 to 16	0.67 to 2	1.5	0.25
Electrical resistance (Ω-cm)	10^{12} to 10^{16}	$> 10^{14}$	3×10^5	10^{15}
Dielectric constant	5.7	9	11	9
Thermal-expansion coefficient ($\times 10^6$ m/m)	1.0	4.0	2.62	6.2
Young's modulus ($\times 10^{10}$ N/m^2)	105	35	17	30
Density (g/cm^3)	3.51	3.26	2.33	3.72

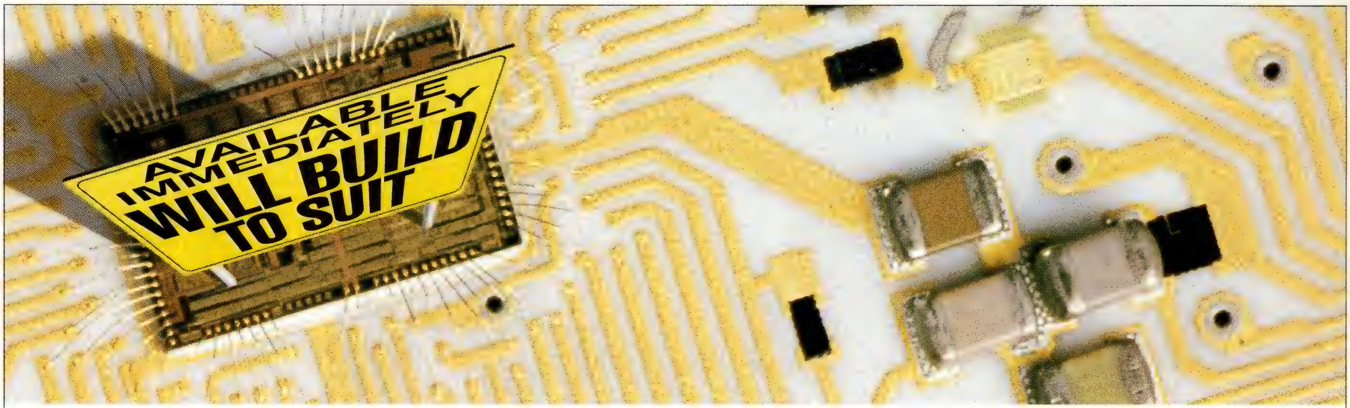
rays of holes in the spacer layers that lie between the diamond substrates to be vertically interconnected. With 0.5-mm buttons in a diagonal square array featuring a horizontal and vertical center-to-center pitch of 1 mm, up to 9765 vertical interconnects fit in a 100-mm^2 spacer board.

Cooling such a structure is no mean feat, and can be achieved with heat sinks at two opposing faces of the cube. With, for example, 1-cm^2 die mounted on a 1.5-cm pitch, each of the 40 substrates in the 100-cm cube might carry 36 VLSI chips, or 1440 chips for the system. If these were 10,000-gate gallium-arsenide (GaAs) chips optimized for speed, they would dissipate about 10 W each or 360 W per board, giving a maximum temperature rise of 22.5°C for the 1-mm-thick diamond substrate. Such a 100-mm cube would contain 14.4 million gates, which is most of the logic in a 16-processor Cray 3 supercomputer.

Advances toward more reliable metallization of synthetic-diamond substrates have been made at the University of Arkansas, Fayetteville. Researchers there have determined that gold is the metal of choice because of its superior conductivity and ease of deposition. But because gold adheres poorly to diamond, an evaporated metallization system of gold and chromium was employed that improved the layer's stability. The evaporated gold-chromium metallization proved more stable than sputtered films of gold and titanium; gold, titanium, and wolfram; or even sputtered gold and chromium.

These and other MCM-related developments are being presented at this week's International Conference and Exhibition on Multichip Modules in Denver. Next year's MCM conference will also be held in Denver from April 13 to 15.

DAVID MALINIAK



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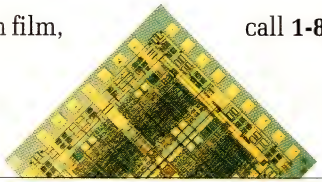

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ELECTRO/93 TAKES ON A HIGH-TECH PROFILE

DAVID MALINIAK

WHILE SESSIONS RANGE FROM NEURAL NETWORKS TO CONCURRENT ENGINEERING, EXHIBITS FOCUS ON SMT AND TEST.

Achievements in high-end technology will attract much attention during the technical conference at this year's Electro. An entire subject track is devoted to the hottest advanced technologies, including artificial neural networks, HDTV, DSP development tools, lightwave communications, and virtual reality. In addition, two concurrent events, SMT/Electro and Test/Electro, will focus on surface-mounted technology and electronics testing, respectively.

The show, which runs from April 27 to 29, will be split between the Raritan Center, Edison, N.J. (Electro), and the Garden State Convention Center, Somerset, N.J. (SMT/Electro and Test/Electro). Electro's technical program spans 29 sessions, while Test/Electro adds comprehensive sessions and tutorials in such areas as boundary scan and built-in self-test; and analog, digital, mixed-signal, and software testing techniques. SMT/Electro will present 16 full- and 5 half-day courses on various SMT topics.

Artificial neural networks (ANNs), which are the subject of two Electro sessions, are wending their way into many applications and have become the subject of a great deal of research *(see "Neural Networks Are Ready For Prime Time,"* ELECTRONIC DESIGN, *Feb. 18, p. 51).* But many researchers feel that ANNs alone aren't always enough, and they continue to explore hybrids composed of neural nets and other techniques like artificial intelligence and fuzzy logic.

In an overview of state-of-the-art ANN hybrid systems, Prof. Robert Hong of the State University of New York (SUNY) at Stony Brook, Syosset, N.Y., highlights some of the weaknesses of ANNs when applied to real-world problems and examines how hybrid approaches can help. For instance, by combining aspects of fuzzy inference with the flexibility and trainability of ANNs, it's possible to form networks that embed prior knowledge and yet can be trained for more optimal behavior or to adapt to a changing environment. A particularly attractive feature of a hybrid system is that it's much easier to obtain reasonable performance from it than it is from a pure ANN, asserts Hong.

Beyond the discussions of ANN research and the promise of hybrids, other papers detail some practical applications of neural networks. For instance, C. James Li and Xueli Yu of the department of mechanical engi-

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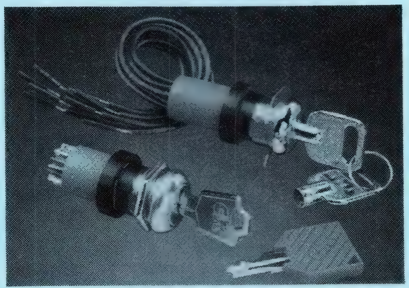

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■ *Booth 2119*

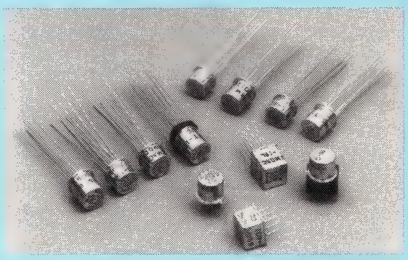
neering, Columbia University, New York, N.Y., will describe their implementation of two small feed-forward neural networks to infer the status of a high-pressure air compressor. When tested with new data that hadn't been seen by the networks before, the networks compiled correct diagnoses for compressor fault conditions at rates of up to 98%.

Another area that's seeing greater practical implementation is digital-signal processing (DSP). But as the DSP market expands and development time shortens, the need grows for a completely integrated design-and-development environment. The newest generation of integrated DSP tools enable designers to create complete signal-processing systems from block diagrams, while the availability of C compilers gives designers the ability to program DSP ICs in a high-level language.

In an evolution paralleling that of microprocessor development environments, DSP tools are often too diverse to work well together. As a result, DSP development is typically highly resource-intensive and all too often fails to yield a salable system. In a paper detailing a graphical approach to design and development of DSP systems, Andrew Jay Krassowski, Star Semiconductor Corp., Warren, N.J., describes how the SPROClab development system simplifies the creation of DSP systems.

MINIATURE RELAYS, CONTACTORS HANDLE HIGH-POWER SWITCHING

A series of high-reliability contactors and a combination solid-state and electromechanical device that offers high-voltage and high-current switching in a compact package are now available. The contactors can handle high-power switching applications ranging from military launch systems to large motors and pumps. Three initial series include a 200-A version that meets MIL spec MS24142 and 100- and 50-A versions. The combination solid-state and electromechanical device will economically replace larger, heavier switching devices three to four times its size. The device features arcless operation, which eliminates carbon buildup on the contacts and increases the unit's useful life. Also shown are the company's miniaturized TO-5 and Minigrid relays. Call for pricing and delivery.



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The SPROClab system uses Star's proprietary multiprocessor IC; an evaluation board; and software for building, debugging, and tuning of signal-processing products.

In turning to the C language for their programming needs, DSP application developers are finding that digital-signal processors have outgrown their former roles as coprocessors. Then, assembly language was sufficient for their programming. In her paper on programming DSPs using C, Sheri J. Bernstein, Intermetrics Inc., Cambridge, Mass., declares that C overcomes the limitations of assembly language that make it necessary to completely rewrite the code to port it to a different hardware platform.

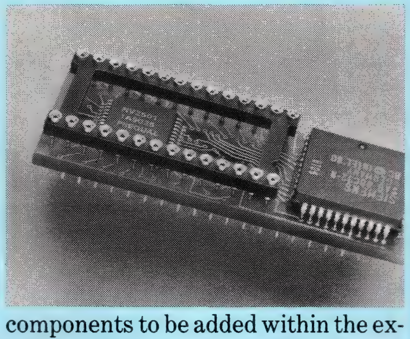
C does have its limitations for DSP programming, however. ANSI-C doesn't support DSP constructs, such as fixed-point numbers, complex numbers, or circular buffers. Likewise, there's no provision for multiple data memories, and no ability to specify on-chip versus off-chip memory. Meanwhile, assembly language still has its place in DSP programming, Bernstein asserts. DSP hardware is often designed with compact, highly efficient instruction sequences in mind for the core algorithms. Any departure from these sequences degrades performance.

The smart approach, therefore, is to use a combination of C and assembly language. This requires a C compiler that can efficiently interface with assembly language. Intermetrics' C compilers support two variations of in-line assembly language, which allow the C programmer to access DSP instructions without the additional overhead of a function call. Thus, C can control the flow of the application, while assembly can handle time-critical algorithms.

Just as competitiveness is an issue for those in the DSP arena, time-to-

STANDARD AND CUSTOM CONNECTORS SOLVE BOARD-DESIGN PROBLEMS

A wide range of standard and custom interconnect products is available to solve board design and rework puzzles. Highlights include the Correct-A-Chip programmed sockets and adapters, which enable users to correct packaging difficulties without implementing expensive board-design changes. The sockets reroute circuit paths to change pinouts within the same package style. With the adapters, users can convert from one termination style to another. For example, surface-mount devices can be substituted on boards designed for through-hole components. The Correct-A-Chip semihybrid daughterboards allow components to be added within the existing socket envelope with no board redesign. Call for pricing.



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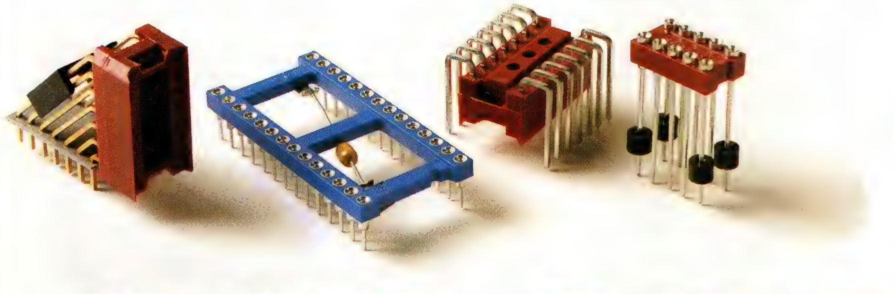

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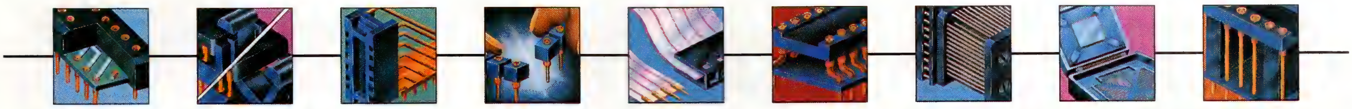

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market has been identified as an overriding concern in the industry at large. In many cases, concurrent engineering is combining with the concept of contract manufacturing to bring about efficient, timely delivery of products. Often, an integrated information system geared to such a manufacturing environment is the key to success.

In a paper regarding the design of an information system for contract manufacturing, Norman J. Viehmann, On-Target Manufacturing Software, Andover, Mass., describes the structure of a seamless on-line information system for contract manufacturing. Viehmann points to relational database-management software and up-to-date computing capacity and speed as the means to providing fingertip control of manufacturing management. By preparing a comprehensive, detailed plan and storing it in an on-line database, managers of manufacturing operations would have complete, current, and accurate information available at all times for decision making.

On-line information systems represent an effort to effectively capture and communicate knowledge. Another approach is proposed by Jerrold Foutz, Rockwell International Corp., Anaheim, Calif., in his paper on hypertext as an enabling tool for concurrent-engineering teams. Information in hypertext can be accessed by a number of paths built in by the author. One can be a conventional, linear path through the information, as if it were plain printed text. But hypertext's advantages reveal themselves when other forms of linkages between the data are used, such as linking by association.

Linking by association mimics long-term human memory, which was the original model for the development of hypertext. By creating paths for various readers, the hypertext author increases the reader's ability to find, absorb, and work with ideas. Linking information in any manner conceivable to the human mind improves retrieval. When combined with networking among team members, hypertext can become a powerful enabler of group processes such as concurrent engineering.

The keys to making hypertext an effective tool for the engineering team lie in several areas. One is to use software with a free or one-time-cost runtime license. Another is to choose a system that permits team members, all of whom must contribute their knowledge to the hypertext, to add information using the tools of their choice. The best hypertext authoring software allows information to be added with any word processor, spreadsheet, database, or computer language. A third key is overcoming the reluctance of engineers to document their work. That reluctance will be compounded if it

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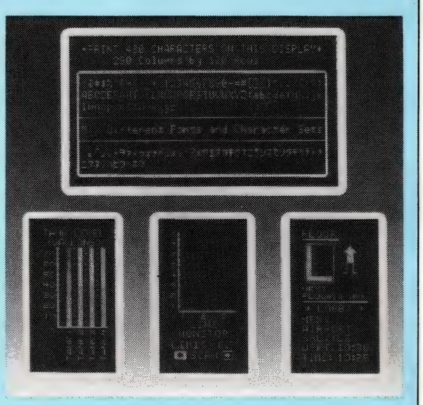
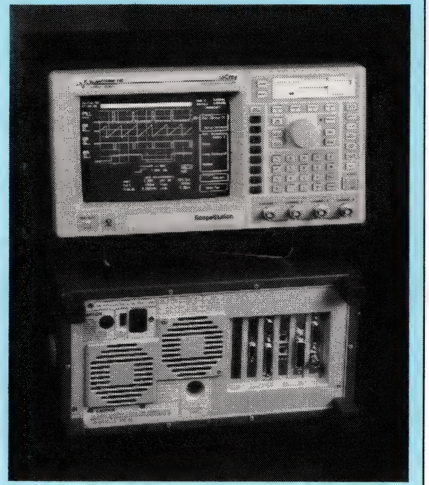
Neon-orange color; flicker-free, bright pixels; a 130° viewing angle; and a 50,000-hour life span are featured in the Plasmadot gas-plasma display. The unit is designed for OEM applications in process-control instrumentation, medical monitors, point-of-sale terminals, alarm and security systems, and more. The display's bright-orange color is more readable and pleasing to the eye than LCD or vacuum-fluorescent displays, and is readily filtered with red, amber, or neutral (gray). Among the display's many advantages is that it can be fabricated with round, square, or rectangular pixel shapes. Pixel sizes range from 0.015 in. minimum to 0.100 in. maximum with inter-pixel spacing as little as 0.100 in. The various available sizes include 128 by 32, 128 by 64, and 280 by 120 pixels. Custom sizes range up to 18 by 24 in. Call for pricing and delivery.

Cherry Electrical Products, 3600 Sunset Ave., Waukegan, IL 60087; (708) 662-9200. **CIRCLE 568**
■ *Booth 2247*



PORTABLE DIGITAL OSCILLOSCOPE STRESSES DATA CONNECTIVITY

Extension of the digital oscilloscope's usefulness is the goal of a range of connectivity features for the ScopeStation portable scope platform. The first member of a planned family, the ScopeStation 140, offers optional direct fax output, Ethernet compatibility, and GPIB 488.2 remote interfacing. It also offers spreadsheet, database, and word-processing file formats as standard. The connectivity features are paired with LeCroy's Smart Triggers for capturing complex signals and an auto-test sequencer. The platform offers four full channels, a 100-MHz analog bandwidth, a 200-megasample/s maximum sampling rate, and a record length of 2000 samples/channel. The basic ScopeStation 140, with one of the three connectivity options, goes for under $5000.



LeCroy Corp., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 425-2000. **CIRCLE 569**
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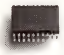
Use TI's innovative TL2218-285 Current Mode Active Terminator.



When applications require fast SCSI designs, use TI's TL2218-285 for performance up to 10 MHz. TI's Current Mode Active Terminator helps assure fast data transmission that's as error-free as you can get. The low (6 pF) output capacitance meets the most demanding SCSI specifications. With our nine-channel devices you can easily implement 18 or 27 (wide) SCSI lines, all without the use of external resistors or capacitors.

A unique current sourcing termination technique provides a constant 24 mA for smoother, faster, single-step transition from low to high *(see graph)*. That's the key to fast, error-free data flow.

And there's more. It is available in TI's advanced thin shrink small-outline package (TSSOP), offers full compatibility with Active Negation Drivers and has a 3.5-V minimum supply voltage. Also included is an on-chip disable function.

TL2218-285 Advantages

- Current Mode Terminator enables operation up to 10 MHz
- Low output capacitance: 6 pF (typ)
- No external components required
- Full compliance with SCSI standards
- Disable function on-chip
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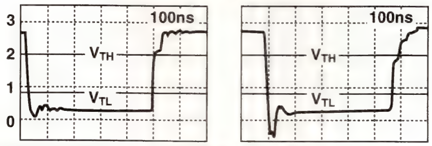

Termination Waveforms

Current Mode Termination TL2218-285

Alternate II Termination

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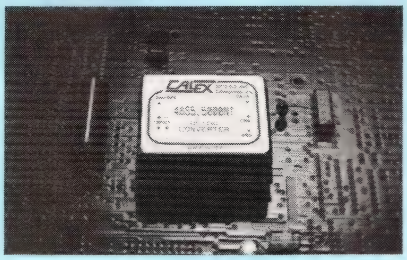
30-W DC-DC CONVERTER MODULES DELIVER 17 REGULATED W/IN.^{3}

Between 25 and 30 W of output power springs from a series of dc-dc converters measuring just 2.02 by 1.62 by 0.55 in. The 48S5.5000NT, 48S12.2500NT, and 48S15.2000NT converters are claimed to be the first to deliver a power density of 17 W/in.^{3} in a package this size. Each has transient-overvoltage suppression diodes at the output terminals. Overcurrent and overtemperature protection are also incorporated as standard equipment. The devices are well-suited for telecommunication applications with a wide 2:1 input-voltage range that covers both the common American and European telecom standards. For flexibility, a trim pin is included to adjust the output voltage. Pricing is $63.45 each in OEM quantities.

***Calex Mfg. Co. Inc.**, 2401 Stanwell Dr., Concord, CA 94520; (800) 542-3355.* **CIRCLE 570**

■ *Booth 2324*



proves time-consuming or difficult to get information translated into hypertext form. It's crucial that training engineers to do so be brief and painless. But once engineers discover hypertext, Foutz asserts, many are unable to imagine how they got work done before they had hypertext available.

The use of enabling technologies in a virtual-enterprise environment is described in a paper by David Reiling of the Southeast Manufacturing Technology Center, the University of South Carolina, Columbia. The paper details the way in which the existing information infrastructure was used to electronically link remote sites throughout South Carolina. The end result of this experiment was to reduce prototyping time for a small manufacturer from 11 weeks to one week. The author expresses his hope that the information superhighway being proposed by the Clinton Administration will make the virtual-enterprise concept more accessible to both large and small manufacturers.☐

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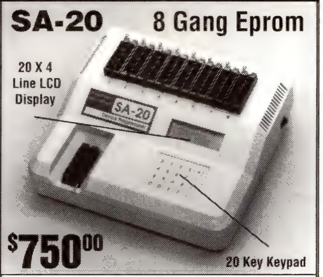

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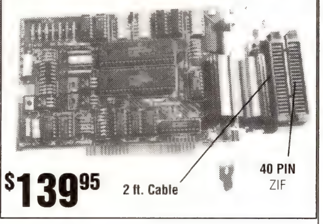

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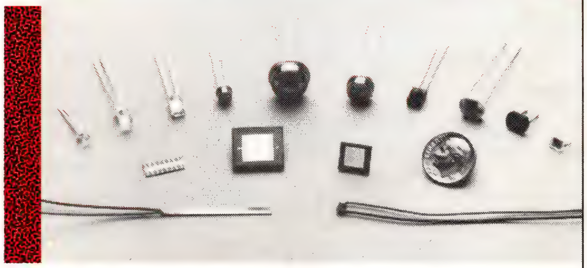

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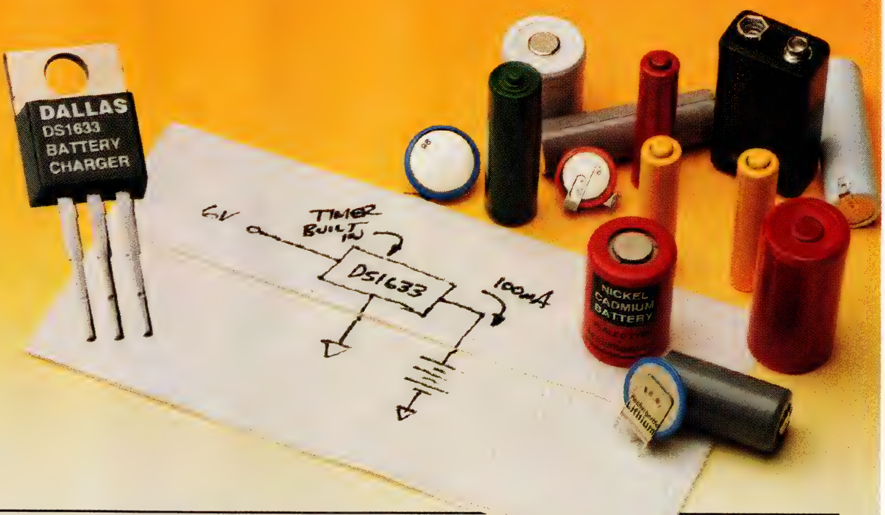
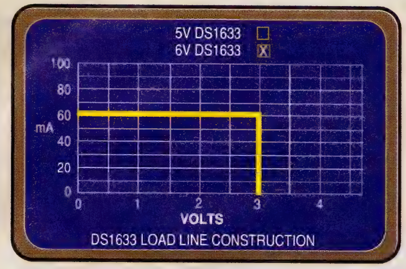
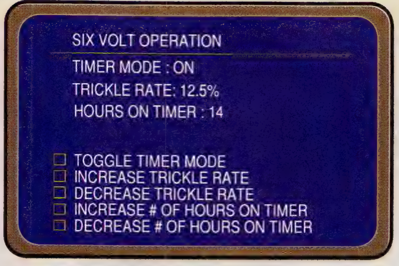
TAKE CHARGE!



3 Steps to Match a DS1633 Battery Charger to Your Battery



1. Draw your charge curve on a PC using the software we provide.

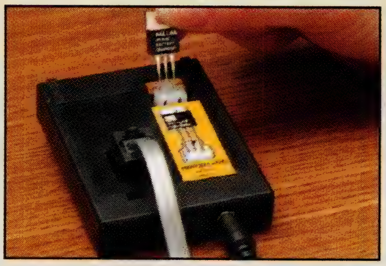


SIX VOLT OPERATION

TIMER MODE : ON
TRICKLE RATE: 12.5%
HOURS ON TIMER : 14

- ☐ TOGGLE TIMER MODE
- ☐ INCREASE TRICKLE RATE
- ☐ DECREASE TRICKLE RATE
- ☐ INCREASE # OF HOURS ON TIMER
- ☐ DECREASE # OF HOURS ON TIMER

2. Set standard charge duration and trickle rate charge with a few mouse clicks.



3. Plug the DS1633 into the programmer and click the mouse. You're done.

Long-term reliability of your rechargeable battery is highly dependent on how well it's cared for. Which is why it makes no sense to use one of those devices that charges your battery right into oblivion.

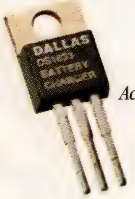
Fast Charge with No Overcharge

Introducing the DS1633, the smart battery charger. It charges quickly but does not overcharge. On power-up, the DS1633 continues to charge the battery at maximum current until it reaches the specified cutoff voltage or charging time exceeds a preset limit. No more batteries killed by over-feeding.

Optimized for emerging 3V systems, the DS1633 can be configured to charge a NiCad one- to three-cell battery pack or a single, rechargeable 3V lithium cell directly at a current of up to 100 mA. With minimal additional components, both the number of cells in the stack and charge current can be increased.

Single-Chip Solution

The DS1633 shrinks all the circuits required for charging into a single, 3-pin, TO-220 package. No external configuration resistors. No capacitors, FET's, or precision voltage references.



Actual Size

Unlike other chargers, which have 16, 20, or even 44 pins that eat up your precious board space, the DS1633 has a mere three pins: a V_{CC} connection to its power supply, a V_{BAT} connection to the battery to be charged, and a ground connection.

Match the Charger to the Battery

The DS1633 is programmed with a template of the kind of battery it is expected to charge. Thanks to this flexibility, you need only inventory one part for a variety of applications. Characteristics such as maximum charging current, charging current with respect to battery voltage, maximum charging time, and level and frequency of trickle charge are all stored in an onboard EPROM memory array. With this programming, the charger is matched to the battery exactly. The better the match, the quicker the charge and the longer the operating life of the battery.

Simplicity Through Software

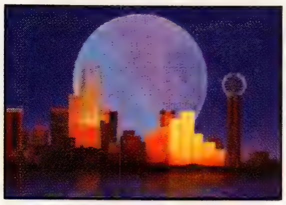
With the DS1633, all the calculations are done for you, so you don't have to make any investment in software development. With the software we provide, you simulate the charger first on the PC and then program the DS1633 with the click of a mouse. After you've made the first one, you can replicate like crazy at a rate of about 10 seconds each.

And in order to make it simpler still, we offer pre-programmed DS1633's that have been tailored to meet the requirements of specific cells and battery pack types.

Take a Test Drive

If you want a quick look at just how easy it is to customize the DS1633 to your application, the DS1633K Battery Charger Kit contains the hardware and software needed to integrate the DS1633 into an application at a very nice price.

For more information on how to take charge of your battery, give us a call.



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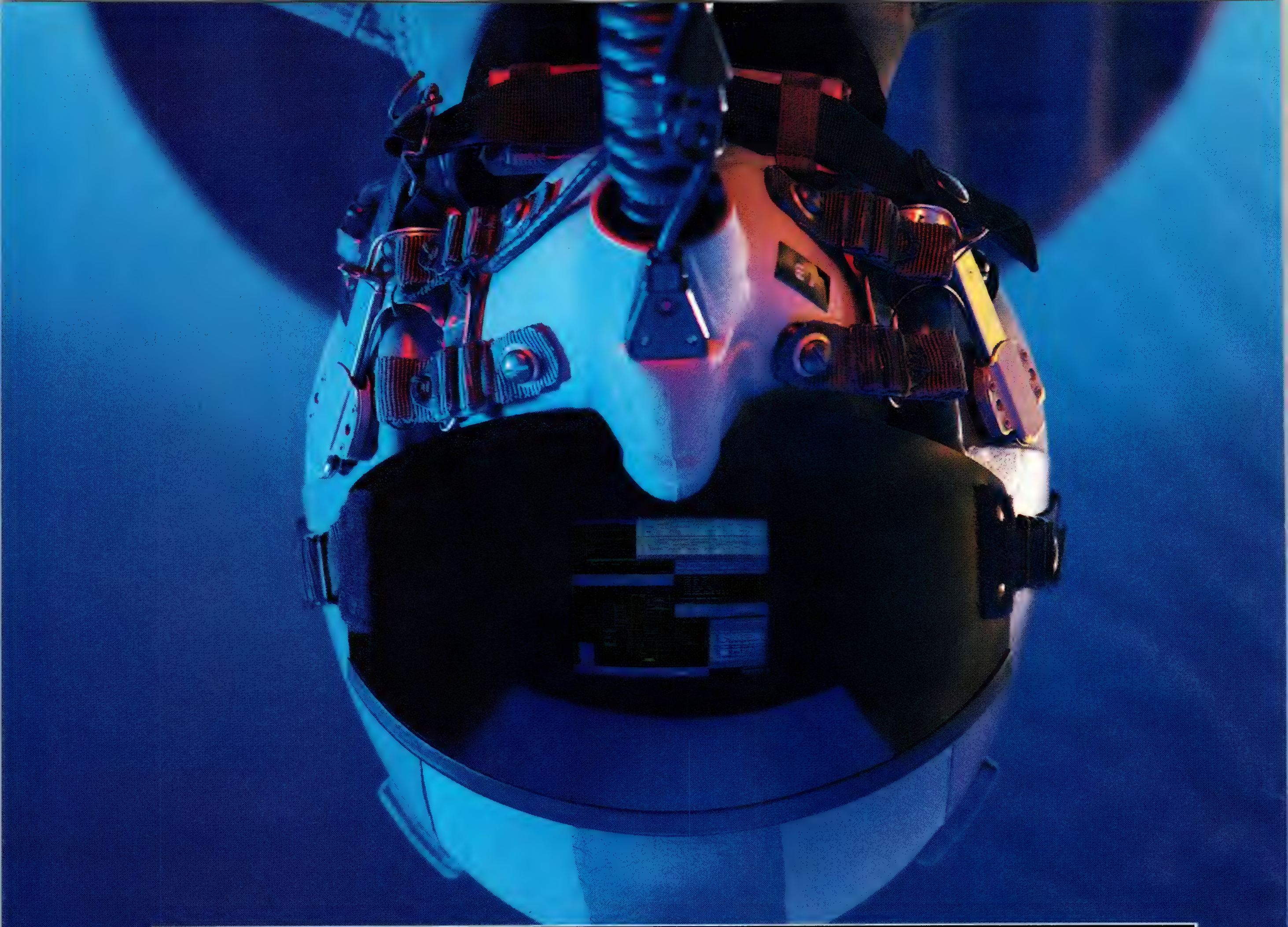

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COMMUNICATIONS CONTROLLER HANDLES NINE PROTOCOLS

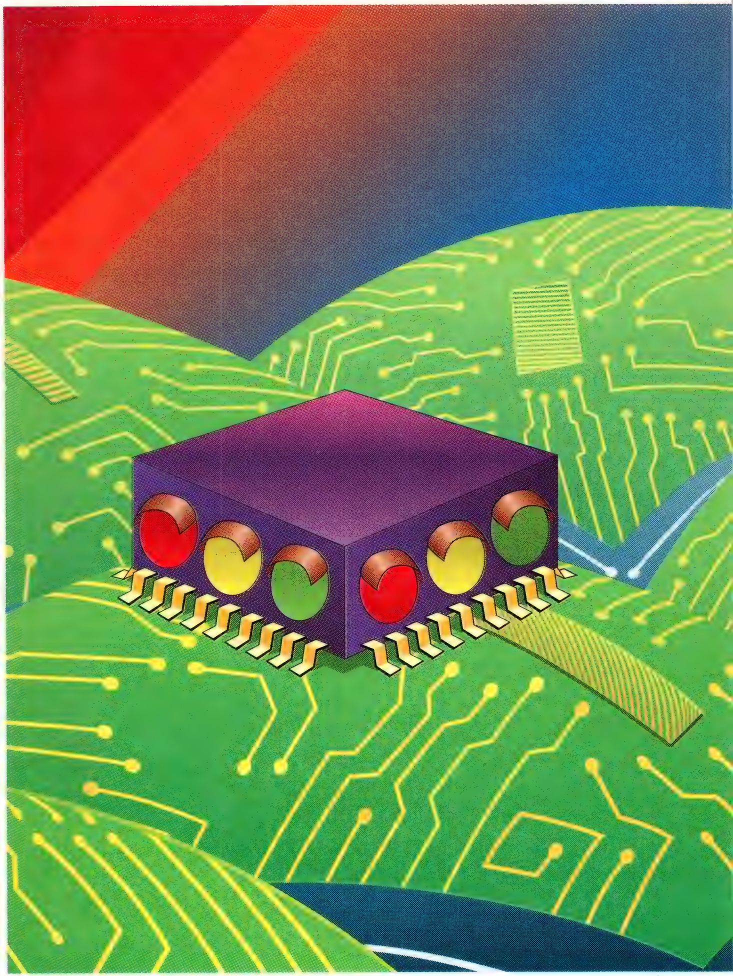
MILT LEONARD

The rise of complex topologies in communications networks has generated many different communications protocols governing the exchange of information between networked elements. Protocols are driven by communications controllers designed into various network elements, such as gateways, bridges, routers, hubs, packet assemblers/disassemblers, data concentrators, and telecommunications and I/O systems. To design such products, the ideal solution would be to use a universal protocol engine that handles all protocols involved in internetworking. Instead, designers of these devices have been stuck with a number of protocol-limited communications controllers from different manufacturers that require the support of dozens of semiconductor chips.

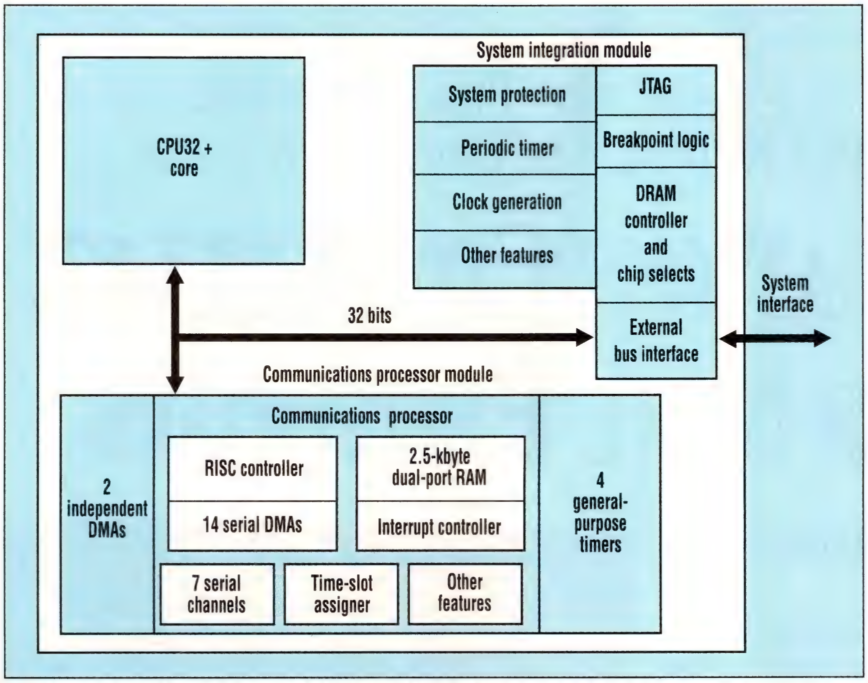
To help simplify the design task, Motorola came up with the MC68360 Quad Integrated Communications Controller (QUICC) multiprotocol engine. The chip integrates an unprecedented level of processing and peripheral functions that Motorola claims is a list of "industry firsts."

The 68360 is the first multiprotocol communications controller to combine local-area-network (LAN) and wide-area-network (WAN) support with a standard microprocessor on one chip. It's also the first to integrate a general-purpose CPU with a time-slot assigner for WAN applications. Available in a 241-pin PGA or 240-pin plastic quad flat pack, the device is also the first to integrate a CPU with Ethernet capability and WAN protocols.

Like other members of Motorola's 68300 Integrated Processor Family, the 68360 has a modular architecture that links the CPU to



peripheral functions with a standard intermodule bus (IMB). The CMOS chip packs a 32-bit general-purpose CPU, a RISC communications processor, four high-bandwidth serial-communications channels that support eight communications protocols, and three low-bandwidth serial communications channels. It also has a time-slot assigner, on-chip memory, and a circuit board's worth of system functions, including DMA and DRAM control



1. THE MC68360 COMMUNICATIONS CONTROLLER integrates all of the circuitry necessary to design internetworking devices, including gateways and bridges. In one bus cycle, the CPU32+ core can operate on 32-bit external operands or read and write 32 bits of data to process higher-layer software-driven communications protocols.

functions *(Fig. 1)*.

When used with the MC68160 Enhanced Ethernet Serial Transceiver (EEST) companion chip, a special version of the controller—the 68EN360—also furnishes Ethernet capability to support a total of nine communications protocols. The two controllers are identical except for the Ethernet interface. The 68EN360 Ethernet version of the controller implements the entire media-access-control (MAC) layer of the IEEE 802.3 standard, except for a serial interface adapter (SIA) and Ethernet transceiver. These functions are provided by the 68160 EEST. It converts non-return-to-zero (NRZ) data from the 68EN360 to a Manchester format for data transmission through an access-unit interface (AUI) for coaxial cable, and the 10Base-T twisted-pair interface through external isolation transformers.

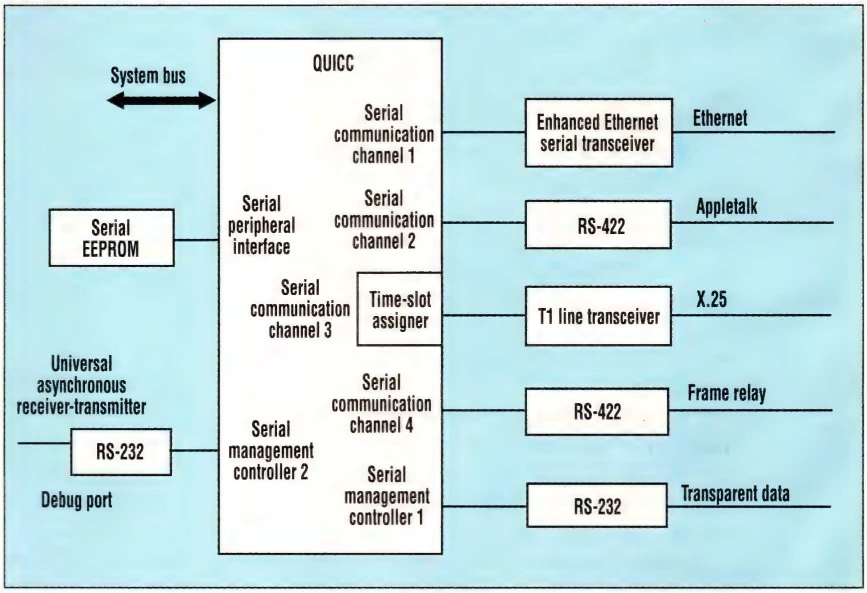
QUICC ARCHITECTURE

Forming the core of the 68360 is Motorola's CPU32+ CPU, which is based on the 68020 microprocessor. The CPU has a 32-bit data bus that can switch dynamically to 8- and 16-bit modes to communicate with 8- and 16-bit peripherals and memory devices. Although its initial clock speed is 25 MHz, a 33-MHz version is being planned. For applications needing even more horsepower, the QUICC can operate as a companion chip to a 68040 microprocessor to get 22-MIPS performance at 25 MHz.

The CPU performs general supervisory functions and software-driven protocol processing. Able to execute an instruction each clock cycle, the RISC communications processor transfers information, handles serial-channel interrupts, and performs built-in protocol-processing functions independent of the core. It also presides over the four high-bandwidth serial communications channels (SCCs).

Each SCC supports a maximum data rate of 2.048 Mbits/s at 25 MHz for American or European T1 transmissions. (T1 transmission consists of 24 channels multiplexed onto one line. The American standard specifies a 1.544-Mbit/s transmission rate; the European standard calls for 30 channels and a 2.048-Mbit/s rate.) With one SCC in the 68EN360 Ethernet version serving as a 10-Mbit/s Ethernet LAN controller, the chip's maximum aggregate full-duplex data rate is 11 Mbits/s at a clock frequency of 25 MHz.

Each SCC operates independently of the others and can handle eight different user-selectable protocols at any given time. Facilities for low-


System bus
QUICC
Serial communication channel 1
Serial peripheral interface
Serial communication channel 2
Serial EEPROM
Serial communication channel 3
Time-slot assigner
Universal asynchronous receiver-transmitter
Serial communication channel 4
Serial management controller 2
RS-232
Debug port
Serial management controller 1
Enhanced Ethernet serial transceiver
Ethernet
RS-422
Appletalk
T1 line transceiver
X.25
RS-422
Frame relay
RS-232
Transparent data

2. ARCHITECTURAL VERSATILITY enables the MC68360 to link a variety of network types. To illustrate, this general-purpose application connects one of the chip's serial communications controllers to Ethernet through the MC68160 transceiver, and another to AppleTalk through an RS-422 device. A third serial channel is linked to an X.25 network through a time-slot assigner, and a fourth channel connects to a frame-relay line through an RS-422 device.

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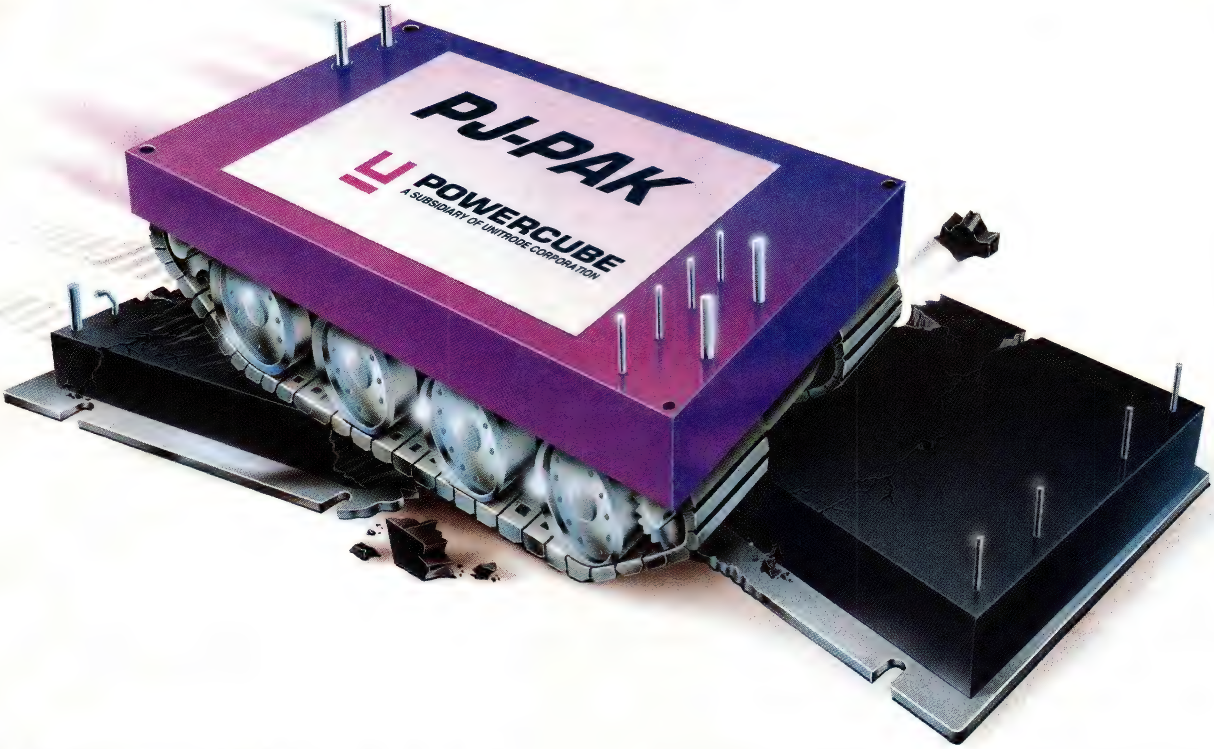
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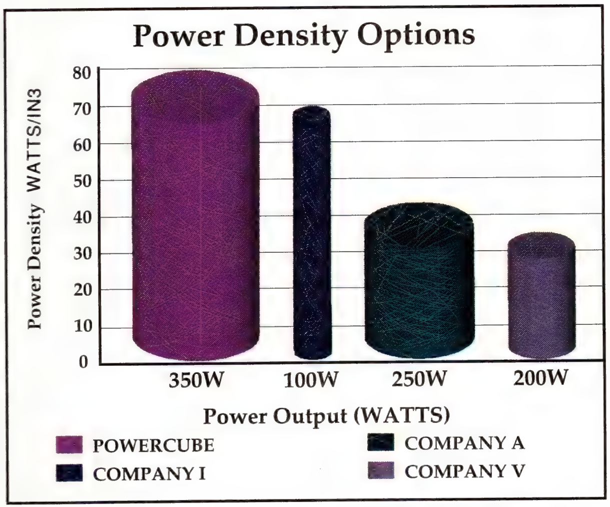

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er-level protocol processing are microcoded in the RISC processor.

Among the protocols supported are the HDLC/SDLC (high-level data-link control/synchronous data-link control), HDLC Bus, SDLC, UART/Synchronous UART (universal asynchronous receiver-transmitter/synchronous UART), BiSync, Signalling System #7 (SS7), Ethernet, LocalTalk, and a Transparent Mode *(see "Some basic facts about protocols," below)*.

Support is given for additional protocols in the form of microcode packages for loading into the controller's dual-port RAM. The microcode operates the RISC communications controller chip.

Specialized protocols and applications that don't require protocol handling can take advantage of QUICC's transparent mode. For example, the 68360 might be used as a controller in a cellular-telephone base station. Thus, communication channels dealing with only raw voice signals could operate in the transparent mode. This mode is also useful where specialized protocols must be implemented in software.

Because these processing-intensive low-level protocols are so pervasive, Motorola elected to implement them in fast hardwired circuitry that runs with the independent RISC processor. Higher-layer protocols are controlled by software running on the chip's CPU32+ microprocessor. Users can design their own software for proprietary upper-level protocols, or use software modules available from Motorola and third-party vendors. Such standard protocols include LAP-B (link-access protocol, balanced), LAP-D (link-access protocol, D channel), and the X.25 packet-layer protocol.

In addition to the four main serial channels, the QUICC furnishes two serial management controllers (SMCs) and one serial peripheral interface (SPI). The SMCs can perform framing and serial interface tasks in ISDN (Integrated Services Digital Network) applications. They can also act as UARTs or as transparent channels. The SPI enables synchronous communication between the 68360 and other Motorola system components, including voice codecs, real-time clocks, microcontrollers, and digital-signal processors. A parallel port on the device supports additional functions, such as a fast interface between multiple QUICCs or a Centronics-printer interface.

Part of the 68360's 2.5-kbyte dual-port RAM serves as a memory-mapped register bank through which the CPU communicates with the serial channels and system-integration functions. The remaining space is available as general-purpose memory and for communications-

SOME BASIC FACTS ABOUT PROTOCOLS

Protocols for communications networks govern the way the various networked elements package, address, transmit, deliver, and interpret data. A protocol controls how a data-sending device encodes the information, attaches special bits for error detection, addresses the data packet, and so on. Data-receiving devices unpack the data, correct transmission errors, and acknowledge receipt of the transmission according to the same protocol.

Protocols are categorized according to the seven-layer ISO (International Standards Organization) Open Systems Interconnect (OSI) reference model. Protocols describing the electronic process of transmitting data—such as plugs, wires, and signal-voltage levels—fall into OSI Layer 1, the physical layer. An example of this is the RS-232C serial interface standard. Layer 2 standards (HDLC and SDLC, for instance) specify data-packaging formats for transmission. Typically, data is packaged as a series of blocks or frames, with each frame containing bits representing user information, message start and finish, destination address, and error correction. HDLC is commonly used in a variety of WANs.

SDLC is a related data-packaging protocol used in IBM SNA (Systems Network Architecture) networks. HDLC Bus is an enhancement of HDLC that allows HDLC-based LANs and other HDLC point-to-multipoint communications to be implemented with ease. UART and Synchronous UART—serial protocols involving universal asynchronous receiver/transmitter devices)—are used by terminal-to-host networks for point-to-point communications between computers and peripherals. BiSync is used by many IBM terminal-to-host networks. Signalling System #7 is used for signaling in telephone-switching systems.

Ethernet is the most widely used LAN standard. The LocalTalk protocol is one way to implement the lower layers of Apple Computer's Appletalk LAN standard. Appletalk can also run on top of Ethernet and token-ring protocols. LocalTalk requires an embedded clocking signal in the transmitted information. The 68360 supports this requirement with a built-in digital phase-locked loop, allowing the clocking signal to be coded and decoded.

Higher-layer protocols define procedures for message routing, error correction and recovery, and initiating and terminating network connections. Examples of these are X.25, TCP/IP (transmission control protocol/internet protocol), and SNA.

A communications controller in a networked device must understand and implement one or more network-specific protocols. When sending data, the controller must partition the data into frames of specified length and add the necessary control information. In the receiving mode, the controller must strip out the control bits and forward the data to the appropriate computer application. In internetworking devices (bridges and gateways), the controller translates between different protocols to convert data from one network into a form suitable for another.

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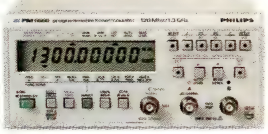

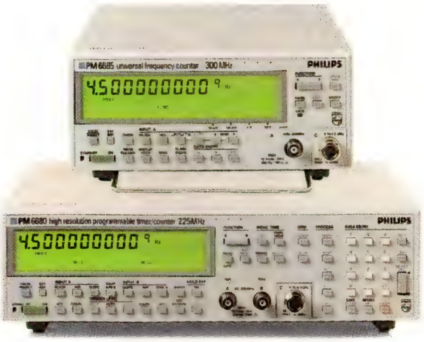
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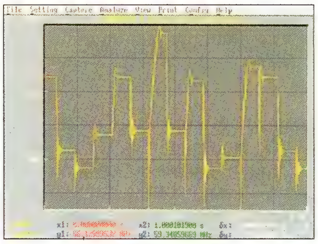

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buffer descriptions.

One of the controller's novel features is a time-slot assigner (TSA), which allows the chip to mix data from the SCCs and SMCs into a time-division multiplexed channel, like that used for T1 and CEPT (Conference for European Post and Telecommunications) transmissions *(Fig. 2)*. The TSA can allocate time slots to any of the controller's SMCs and SCCs. It can also work with either bit- or byte-sized chunks of data and simultaneously support two multiplexed links, such as a T1 and CEPT connection.

SYSTEM SUPPORT

One chip module contains various functions that are commonly used in system integration. Memory-related functions of this system-integration module (SIM) include a glueless interface to eight banks of external DRAM, SRAM, EPROM, EEPROM, and other memory devices. The module's DRAM controller not only supervises DRAM operation, but also provides a direct interface to a 68040 microprocessor. This feature is valuable in high-performance systems using a 68040 microprocessor as the host processor and the 68360 as a peripheral. The module's two independent DMA controllers supply external system devices with their own direct access to memory.

The SIM also has an interrupt controller that can handle 32 prioritized-interrupt sources, 4 general-purpose timer-counters, software and hardware watchdog timers, a periodic interval timer, and 16 RISC-based timers. Also included is a clock generator that can synthesize a clock signal from a low-cost 32-kHz crystal. A low-power standby mode is provided for applications powered by phone lines or batteries. Full operation is possible from dc to 25 MHz. Other SIM features supporting system integration include built-in test features compatible with the JTAG boundary-scan specification (IEEE P1149.1), and on-chip hardware breakpoints.

CONNECTING TO ETHERNET

In addition to the glueless interface with the Ethernet controller contained in the 68EN360, the 68160 EEST chip links with other standard Ethernet LAN controllers, including those available from Advanced Micro Devices, National Semiconductor, Intel, and Fujitsu. Prior to twisted-pair data reception, the chip's squelch circuitry qualifies input signals for correct amplitude, pulse-width, and sequence requirements. Other chip functions are driver pre-emphasis for twisted-pair output data, digital-phase-locked loop timing recovery and data decoding, transmit and receive status, output collision detection and status output, twisted-pair jabber detection and status output, and link-integrity testing and status output.

Furnished in a 52-pin quad flat pack for surface mounting, the 68160 also offers a variety of user options for more complete functionality. Among these options are: automatic wiring-polarity fault detection and correction for twisted pair wiring, automatic port selection with status output, a crystal-controlled clock oscillator or an external clock generator, a signal-quality error test for twisted-pair wiring, a diagnostic local-loopback testing capability, and full-duplex operation on twisted-pair wiring.

Motorola supplies an application development system for evaluating the 68360 and for debugging target systems. The kit includes a circuit board for use with a dumb terminal, and an IBM PC or a Sun 4 computer. A board-resident debugger allows detailed evaluation of system software. Other development tools, such as emulators, are available from third-party vendors.☐

PRICE AND AVAILABILITY

The MC68360 QUICC controller costs $49.90 each in quantities of 10,000. The MC68EN360 Ethernet version sells for $59.90 each in the same quantity. The MC68160 EEST costs $10.00 each in quantities of 10,000. All chips will be available the second half of 1993.

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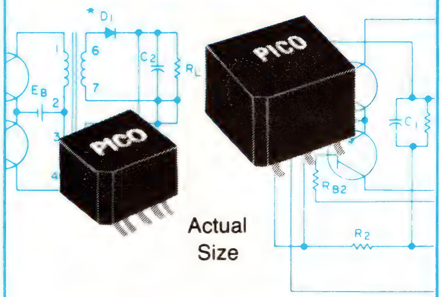

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A REVOLUTION IS IN STORE FOR FLAT-PANEL DISPLAYS

Emerging Technologies Using Existing IC Fabrication Plants Will Deliver Significantly Higher Resolution At Lower Cost.

BY JACK SHANDLE

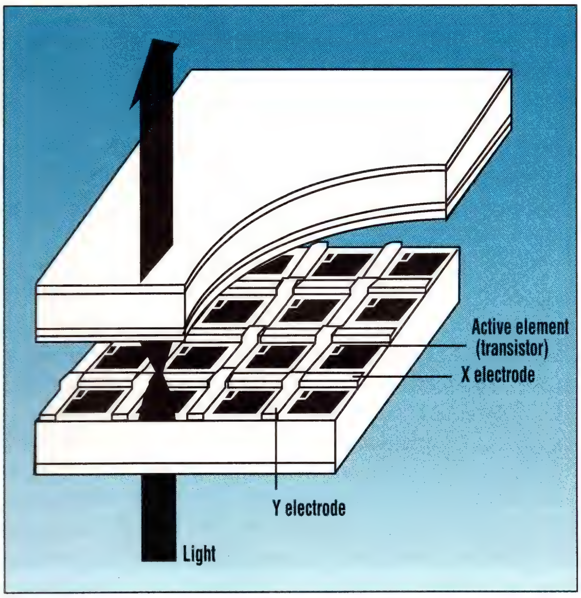
The once-stable world of flat-panel displays is about to become unhinged. Beginning in the next two months and proceeding through the next two years, a steady march of new technologies is highly likely to make in-roads into the territory now dominated by amorphous-silicon-based liquid-crystal displays (LCDs). The most prominent challengers include technologies that leverage the existing silicon-IC manufacturing infrastructure with either single-crystal silicon or polysilicon instead of amorphous silicon.

Progress is also being made in what are now niche technologies, particularly plasma-discharge and electroluminescent displays. At the same time, conventional amorphous silicon technology is being flogged by market leaders like Sharp Electronics Corp., Tokyo, Japan, to produce better display performance and higher yields. While the outcome of the struggle for market position is uncertain, we can be sure that over the next two years, the technology will undergo rapid improvement thanks to competition from both within and outside the conventional flat-panel-display community .

Of all the innovation underway, single-crystal-silicon developments are potentially the most exciting because they represent a technology dislocation for the flat-panel-display industry. The ability to fabricate LCDs using single-crystal silicon, which is also known as x-Si, will usher in a paradigm shift for systems manufacturers. The march toward larger and larger direct-view displays produced on dedicated manufacturing lines will be challenged by small displays exhibiting very high information density and lightning-fast switching speeds. With these characteristics, the new displays can be positioned close to the user's eye for portable computing applications to create something resembling a virtual-reality environment.

Applications that require large screens can use projection displays that have very high resolution. This includes desktop workstation monitors with resolution equaling or superior to the best that CRTs offer, but without the bulk or high-voltage problems. Instead of dedicated production lines, the new active-matrix LCDs (AMLCDs) and field-emission displays (FEDs) would be manufactured using the existing IC-wafer fabrication infrastructure. Instead of ever-increasing complexity and low yields, flat-panel displays would follow the same cost-reduction curve as silicon ICs.

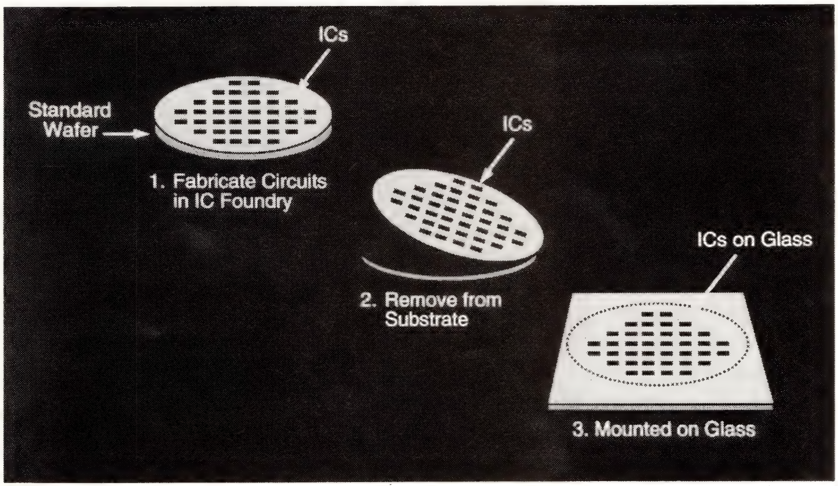
One problem for amorphous-silicon displays is low yield caused in part by the thin-film transistors (TFTs) integrated into AMLCDs *(Fig. 1)*. They're called active-matrix displays because each pixel



1. Conventional active-matrix LCD technology eliminates screen flicker and increases pixel time response by fabricating a thin-film-transistor on each pixel to turn it on and off. Although this makes for a more effective display, it is a major reason why yields are low.

can be addressed (or switched) by the TFT rather than addressing an entire row, which is the technique in passive-matrix LCDs. A non-functioning TFT inactivates the pixel it controls, and very few bad pixels can be tolerated in a computer-system display. By using standard IC processing techniques, x-Si should substantially increase yields.

Arguably, an even more important advantage of using x-Si is that logic circuits can be fabricated on the display's periphery. Amorphous-silicon-based technology requires that the column and row driver circuits that control the pixels be bonded to the display. This chip-on-glass technique limits line densities to about 150 lines/in. Fabricating these drivers on the same x-Si wafer as the pixels delivers a 10-fold increase in line density, but that's just the beginning. Instead of residing on an adapter card or motherboard, complex circuits can also be fabricated on the display's surface. In the future, much of a computer's circuitry could be on the display panel. "The vision being whispered around is a computer in your eyeglasses," says John C. Fan, president of Kopin Corp., Taunton, Mass. "It is portable computing that includes speech recognition and wireless communications."



2. Wafer-engineering techniques, adapted by Kopin Corp., make it possible to transfer a very thin, single-crystal silicon film (containing relatively complex circuits) from the silicon crystal to a glass or plastic substrate. The substrate forms the carrying vehicle for the electronics and liquid-crystal material.

Many of the same arguments that can be made for x-Si apply in a somewhat diminished extent to polysilicon. Researchers at the Xerox Corp.'s Palo Alto, Calif., Research Center (PARC), for example, have fabricated digital-to-analog converters (DACs) in polysilicon, says Malcolm Thompson, director of the Electronics and Imaging Laboratory at Xerox PARC. Amorphous silicon technology is also being pushed to deliver higher performance. Although its low-electron mobility and nonlinear performance make it unsuitable for complex ICs, the information density of the latest amorphous-silicon prototypes is impressive. Xerox PARC will deliver a paper at the Society for Information Displays (SID) Conference next month, for example, that describes an amorphous-silicon-based, 13-in.-diameter, active-matrix display that integrates 6.3 million pixels, says Thompson.

The main question regarding active-matrix, amorphous-silicon displays, however, continues to be yield. Being able to make a prototype is far different from manufacturing 1000 a day, and the same could be true for the new technologies that have yet to reach the production stage.

The fast switching speed of x-Si displays can also impact industries where human vision isn't involved. In these applications, the display becomes a massively parallel output device for optical computing. "Machine-vision people are very interested in this technology" notes Fan. "The idea is to use charge-coupled devices (CCDs) as the receiver." Liquid-crystal materials become the limiting factor in using a CCD panel as the transmitter, however, and this will prompt a move to ferrocrystal materials.

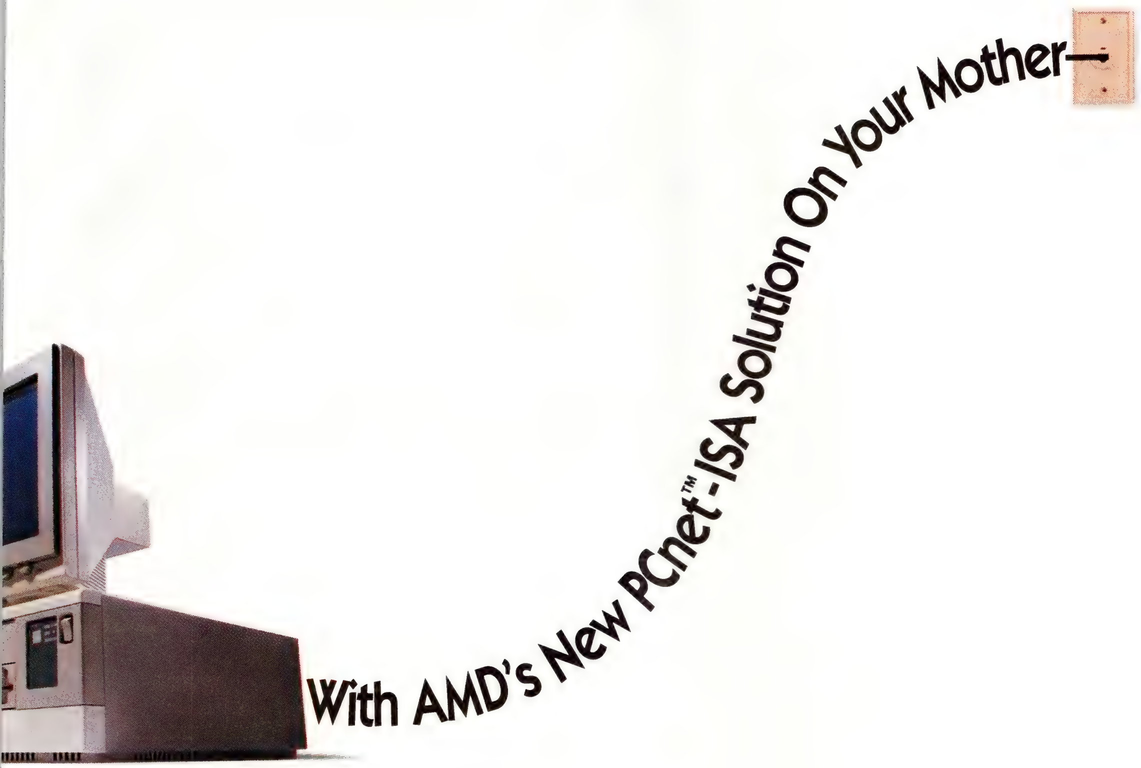
While the inherent advantages of x-Si over amorphous silicon and polysilicon have always been acknowledged, a means of somehow getting the circuits integral to the display onto the glass panel has been elusive. These circuits include row and column drivers and TFTs for AMLCDs. Beginning in the mid-1970s, research laboratories around the world worked on the problem for about a decade without coming up with a solution, says Kopin's Fan.

"In 1984, the Japanese concluded that it probably could not be done. So they froze the technology with amorphous silicon and began to drive it." Meanwhile, Fan and others from the Massachusetts Institute of Technology founded Kopin in 1984 as a wafer-engineering consulting company (besides its consulting work, Kopin sells wafer-engineered materials to leading-edge companies, such as Rockwell International, Texas Instruments, and Boeing).

In 1991, Kopin initiated an aggressive program to leverage its wafer-engineering expertise into x-Si-based AMLCDs. The company came up with a transfer technology it calls Smart Slide, in which a thin film containing the circuits is moved from the wafer to the glass where the thin film is attached with an adhesive. Late last year, Kopin signed on Rockwell as a partner in manufacturing AMLCDs using the new technology. The Smart Slide name refers to the transparent nature of the thin strip of silicon containing the circuits, which is reminiscent of a 35-mm slide. The term Smart Slide is used because the process includes circuit "intelligence."

THIN-FILM TRANSFER

Fan will not disclose details of the transfer process, largely because "it's easy and low cost to do if you know the tricks," he says. The film containing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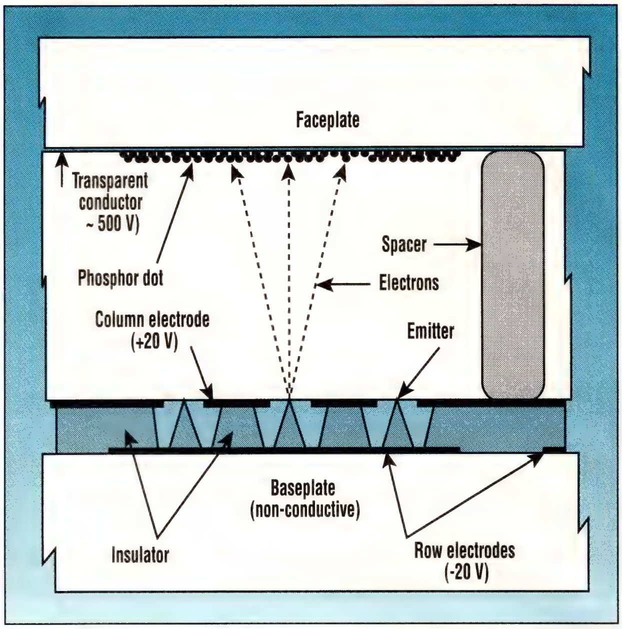
the circuits is usually less than 0.5-μm thick and 5 to 6 in. in diameter, depending on the size of the wafer *(Fig. 2)*. The same process that's used for glass panels is just as applicable for plastic panels, which will make a more-mechanically robust display for hand-held-computer applications.

Kopin has successfully transferred RAM and gate arrays without decreasing yield, he says. Yield ranges between 80% and 90%, depending on the particular silicon process being used. More complex circuits like microprocessors and high-density DRAMs require very tight uniformity for the transistors, and these types of circuits are not being contemplated at this time, asserts Fan.

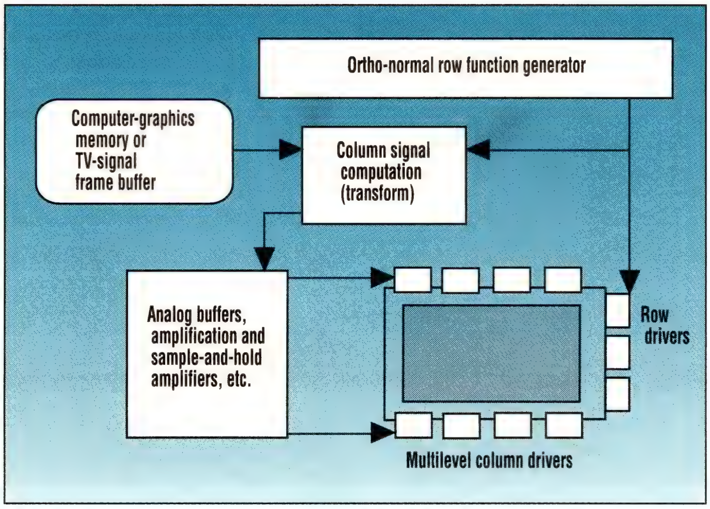
The transfer technique process developed by Kopin begins with a silicon-on-insulator (SOI) material created with the company's Isolated Silicon Epitaxy (ISE) process. The devices to be transferred are fabricated on a thin film of x-Si on top of the buried oxide layer created by the ISE process. This step—fabricating the devices—uses conventional IC processes and will be done by third-party foundries. "We do not ask them to do anything different other than perhaps change their implant schedule," says Fan. The wafers are sent to Kopin for the proprietary transfer processing. System yield also includes the assembly process, and although Kopin has no system yield statistics in a production environment, it doesn't anticipate major difficulties.

Sharp Corp. and other leading TFT AMLCD manufacturers won't release yield figures, but they're generally believed to be below 20%. Al Ipri, a researcher at David Sarnoff Laboratories, Princeton, N.J., who has been working with Kopin on prototypes, confirms that yields on Kopin's process are high. "We send them 30 or 40 displays and they all come back perfectly," he says. Ipri doesn't know enough about the Kopin transfer process to say if it can scale economically up to 1000 panels per day, but "the rest of the process is standard silicon and is scalable, as is the material they start with."



3. Field-emission displays are based on extremely small cathodes fabricated on silicon. The cathodes project electrons onto a phosphor when excited by an electric field.

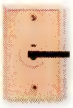
Because silicon wafers are used, the size of any single transfer film is limited to the size of a wafer. The panels can be tiled to produce larger panels. Kopin has prototyped such panels for notebook-size computers, but tiling is expensive, says Fan. Projection systems for large displays are a better solution because of the 10-fold increase in information density compared to today's technology. The primary materials-science reason behind the advantages of x-Si is the well-known physical phenomenon that electrons move faster in x-Si than in amorphous silicon or polysilicon. The electron mobility of x-Si is 500 times that of amorphous silicon and about 15 times faster than polysilicon. Electron mobility has a direct impact on switching speed. And since each transistor in an AMLCD is switched in each frame, switching speed has a pronounced impact on display resolution.


Ortho-normal row function generator
Computer-graphics memory or TV-signal frame buffer
Column signal computation (transform)
Analog buffers, amplification and sample-and-hold amplifiers, etc.
Row drivers
Multilevel column drivers

4. Active addressing of passive-matrix displays will bring screen performance of passive-matrix technology in line with active-matrix LCDs while keeping prices low. Active-matrix addressing, developed by Motif Inc., uses complex algorithms to keep track of the rms voltage at each pixel.

For example, a monochrome 640-by-480-pixel VGA display has about 250,000 pixels that must be switched for each frame, or about one-thirtieth of a second. A 2000-by-2000-pixel display has 4 million pixels to be switched in the same time, which clearly implies an eight-times-faster clock. So, x-Si, which has a conservatively estimated clock of 100 MHz, can run much-faster frame rates than amorphous or polysilicon.

Similarly, x-Si has a pronounced advantage in terms of feature size. The smallest feature size attainable using amorphous silicon is between 5 and 10 μm, says Jack Salerno, Kopin's vice president for dis-



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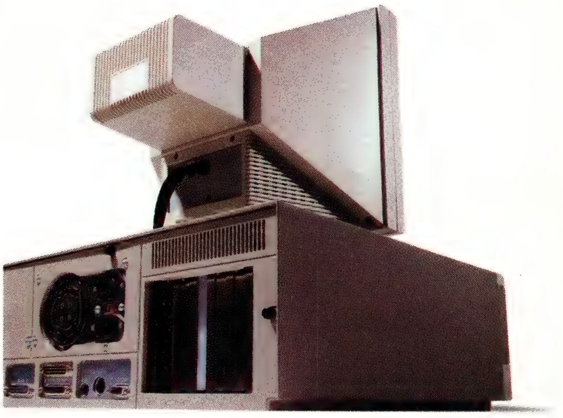

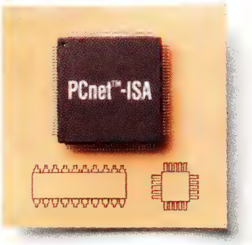

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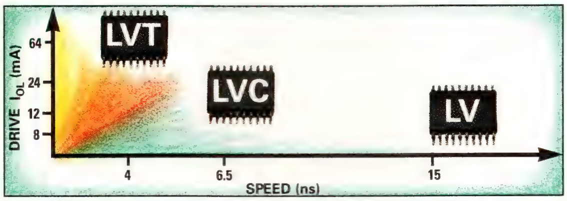

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play products. Polysilicon's smallest feature size is 3 to 5 μm, and x-Si boasts a smallest feature size of about 0.5 μm. There is, however, no intent to go under 2 μm because of the diminishing returns of higher resolutions and the fact that more-expensive lithography equipment is needed for line widths under 1.5 μm.

Small feature size becomes important, says Salerno, when the application requires a half-inch diagonal display that's to be projected onto a 100-in. diagonal screen. Small feature size also has a somewhat unexpected impact on the cost of projection systems. A display with 100 lines/in. resolution produces a poor picture when projected on a large screen. So today's state-of-the-art projection systems use three panels, one each for red, green, and blue color components. Each panel has its own lens. Three images (red, green, and blue) are superimposed on the projection screen to give the projected display an apparent resolution three times greater than a single panel could produce.

The cost implications of the lenses, however, are quite severe. Optics accounts for about 70% of the cost of projection's displays. Kopin's prototype displays, on the other hand, implement such high resolution that only one panel is required, reducing the cost of the associated optics by two-thirds, says Fan. At the other end of the size spectrum, head-mounted displays—which are almost always projected because the image must be made to converge at infinity—require very small physical size with very high information density. Obvious examples of commercial uses include aircraft goggles, but virtual-reality and video-game companies have expressed interest in "computers in eyeglasses," explains Fan. The Defense Advanced Research Projects Agency has awarded Kopin a $9 million contract for a helmet-mounted display.

FIELD-EMISSION DISPLAYS

As promising as Kopin's x-Si-based technology is, however, it's not the only company planning to leverage the existing IC infrastructure to manufacture flat-panel displays. Micron Display Technology, a subsidiary of the DRAM and SRAM manufacturer Micron Technology, Boise, Idaho, is pushing hard to have a working model of a monochrome FED by early 1994. A color version should follow within a year, says Kipp Bedard, a vice president of Micron Semiconductor.

FEDs should achieve roughly the same information density—1000 pixels/in.—as Kopin's Smart Slide technology. But because they produce light by bombarding phosphors with electrons, Micron's goal is to achieve a total brightness level of 1000 foot-Lamberts (fL), which is higher than anything LCDs can offer.

FEDs can best be thought of an array of microminiature cold-cathode CRTs that bombard phosphors with electrons over a very short distance—roughly the thickness of the panel *(Fig. 3)*. LCDs, on the other hand, transmit only 2% to 3% of the backlight that's used to illuminate the display.

The best-known demonstration of miniature cold-cathode technology was shown last year by LETI, a European consortium. However, its original technology forms the cathodes by sputtering metal on a glass plate. Micron and others—notably the Microelectronics and Computer Consortium (MCC) in Austin, Texas; Pixel International, Rousset, France; and perhaps IBM Corp., Armonk, N.Y.—are reportedly working on silicon-based implementations that form the cathode and the grid.

In most respects, FEDs have the same operating characteristics as their CRT cousins: very wide viewing angles, high contrast levels, frame rates that can easily handle video, and very-high-resolution levels. The major differences are that CRTs are heavy and bulky. CRTs are also a hot-cathode technology—the cathode is heated to free electrons, which are directed to their target pixels by electromagnetic fields.

The three major technology challenges in FEDs are the drive circuitry, display integration, and system fabrication, says Dave Cathey, president of Micron Display Technology. Drive circuitry, which will be fabricated on silicon, must use low power. The target specification is to have 100 emitters per pixel, which is expected to deliver a healthy measure of redundancy but could create addressing difficulties for the drive circuitry. Micron won't disclose details about how it will fabricate the emitter cones, so the details of redundancy and addressing technologies remain proprietary.

Another problem is the tendency for electrons to be sprayed out in many directions instead of heading straight for the intended pixel. This has implications for long-term reliability and manufacturability. Surprisingly, Cathey says the lifetime of the emitter tips isn't expected to be a problem because it's a cold-cathode technology that operates in a vacuum. System integration—how the display is put together—poses a problem, he says, because there are lots of interacting factors that aren't readily discernible. Implementing color doesn't appear to be of much concern to Micron. The same phosphors that have been developed for CRTs can be used for small displays, and lower-voltage versions of CRT-type phosphors will be required for larger-area FEDs. But an interim solution may be to use monochrome displays and color filters similar to those used to create color in LCD panels.

Gray scale can be implemented in a number of ways. One method, already used in LCD technology, is pulse-width modulation, in which the number of voltage pulses over a specific time creates the gray scale. Another technique is varying voltage intensity, which is an analog technique used in CRTs. Other methods of implementing gray scale are also being investigated, says Cathey.

FED technology will require a second voltage source besides the standard 3 or 5 V used for sys-

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tem logic, he says. But because it will be very low in current, it doesn't create a design problem and will, in all likelihood, be implemented using an off-the-shelf IC. Since its technology uses standard silicon wafers as a starting point and is somewhat constrained by wafer size, Micron's target markets are similar to Kopin's—high-information-density goggle-type displays and projection displays. Micron will almost undoubtedly follow Kopin into the market, perhaps by a year, if both companies deliver on their development schedules.

BETTER STANDARD LCDS

Kopin and FED proponents like Micron are on their way to developing technologies that offer far-less-sophisticated manufacturing operations than conventional amorphous-silicon-based LCD technologies used by Sharp and other companies already well entrenched in the flat-panel market. But the state of the art is improving in conventional flat-panel displays as well.

Motif Inc., Tualatin, Ore., for example, has announced a technology that might well put passive-matrix displays that use supertwist-nematic liquid crystals—instead of twisted nematic materials employed in AMLCDs—in the running for portable computing applications, without the relatively high cost of AMLCDs. The latter depends on fabricating thin-film transistors on the panel to achieve the benefits of active addressing.

Motif, a joint venture of In Focus Systems Inc., Tualatin, and Motorola Semiconductor Corp., Phoenix, Ariz., has implemented active addressing of passive-matrix displays. Passive-matrix displays have conventionally been addressed by selecting the rows and columns with a single 20-V pulse once each frame. This was fine as long as the display didn't change too frequently. Liquid-crystal material which produced light that decayed slowly after being excited was used to keep contrast relatively constant between electronic refreshes. But when computer displays needed to speed up to show, for example, the travel of a mouse or to draw a graphic window, faster liquid-crystal material had to be employed. Since this material also decays faster, it created problems such as loss of contrast, flicker, and gray-scale noise—a localized flicker or swimming effect in the intermediate gray shades that can be used to create color.

Motif's solution is based on the fact that the switching mechanism of liquid crystals depends upon an rms value of voltage, says Paul Gulick, CEO and chief technical officer of Motif, and on the further observation that the rms voltage need not be implemented with a single pulse. The company's active-addressing scheme provides a continuous voltage on each pixel and gives the pixel just enough more electrical energy when it is to be switched on *(Fig. 4)*. All rows are selected all of the time with special, low-amplitude, bilevel signals.

5. Plasma-discharge displays, like this 30-in.-diagonal prototype, have targeted high-definition TV (HDTV) as a primary future application. The technology can produce a very large, direct-view display that can be hung on a wall. Developed by Photonics Imaging, the prototype has part of the screen blanked because column and row driver circuits are still in development.

Since the only way to deliver a voltage to a pixel is along an entire row, and because the pixels are also being addressed by the column drivers, it becomes a difficult task to keep the rms voltage for each pixel at just the right level. Each row must receive its own characteristic signal. Because each row is simultaneously "selected," the column signal depends on the collective information state of every pixel in the column.

Special algorithms have been developed using digital-signal-processing (DSP) techniques to implement this complex addressing scheme. The result, however, is that close to active-matrix performance characteristics can be achieved—and in some instances surpassed—with passive-matrix displays. These include 30-ms response time, a contrast ratio of 30:1, 64 gray levels, and a palette of 262,144 colors—all at a cost of about one-half of TFT displays, according to Motif.

Full-custom chips to implement active-addressing should be on the market by the third quarter of 1993, says Gulick. They will be fairly large because they require memory segments to store intermediate images. In the initial prototype displays, four ICs will be used to handle a 640-by-480-pixel monochrome display. A 640-by-480-pixel color display would need 12 chips, four for each of the three primary colors. The chips will be placed on the panel along with the conventional driver chips because their role is simply to keep the pixels actively addressed with a specific rms voltage. Motif will sell the chips to a broad range of LCD manufacturers. It will also supply panels to its joint-venture parents, Motorola and In Focus Systems, with production starting in the first quarter of 1994. Physical size will initially be limited to 6-in. diagonals.

Sharp Electronics, which has about a 65% share of the active-matrix market, also continues to make incremental improvements in its technology, says Joel Pollack, product marketing manager for the Microelectronics Group's Display Products division, Camas, Wash. Although Sharp is evaluating other technologies, its commitment to amorphous silicon remains strong, he says.

It is significant that the notebook computer market is not one that either Kopin or Micron mention

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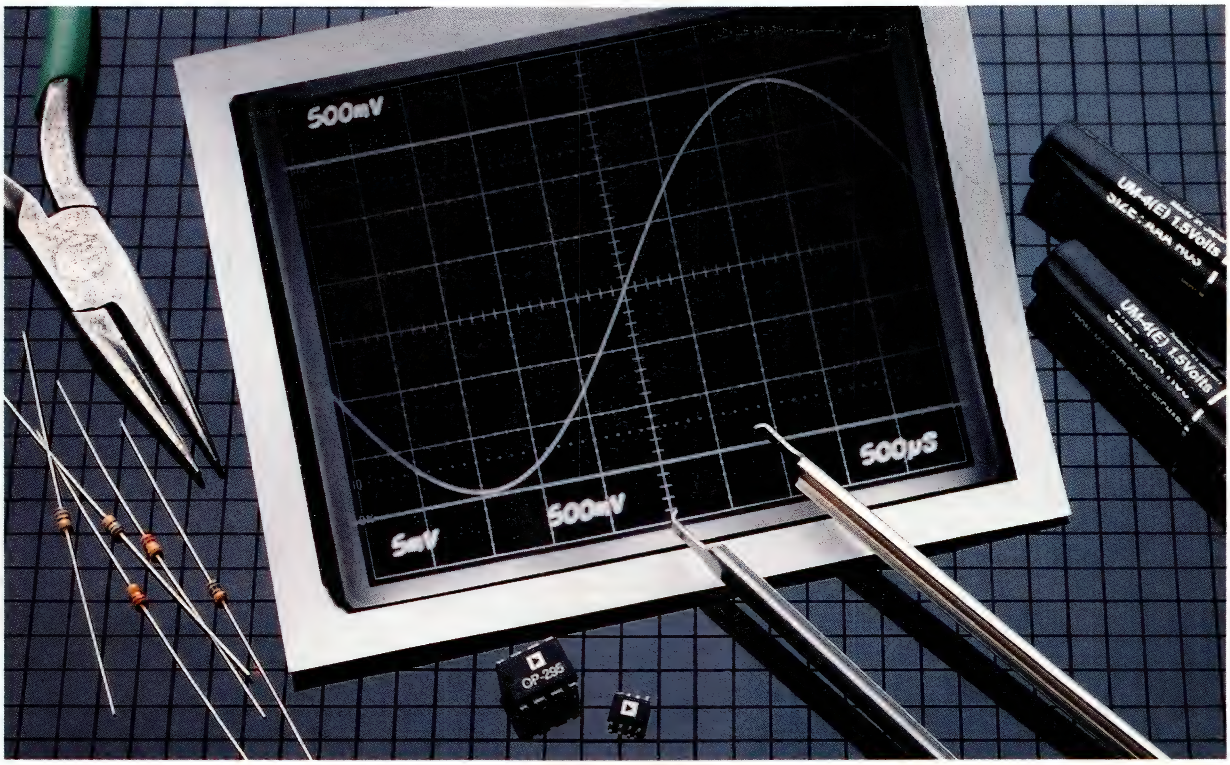

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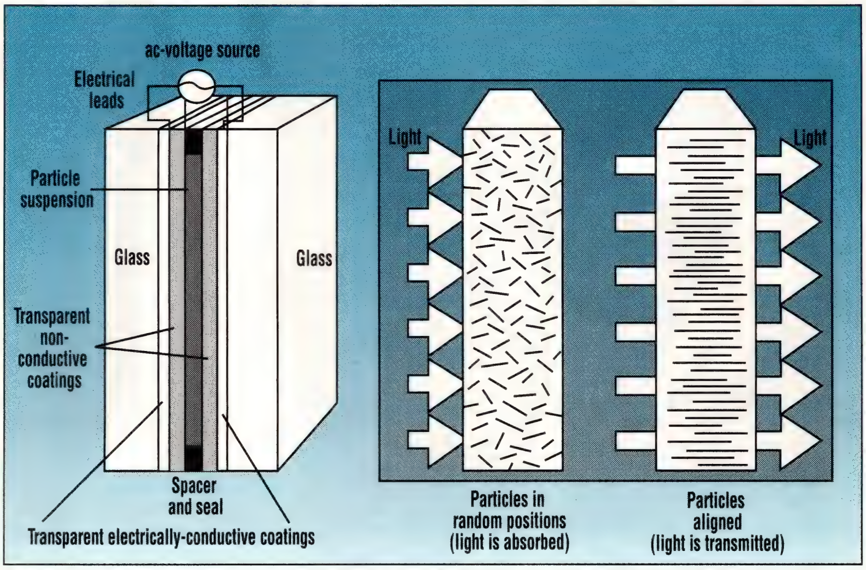
as a top priority. Their technologies are best suited to small, high-resolution displays that might be used in goggles or for large-picture projection screens. Notebook and other intermediate-size displays are likely to remain in amorphous silicon—or perhaps polysilicon—for quite some time.

Sharp can produce a display that delivers 1024-by-768-pixel resolution, says Pollack, but there appears to be little demand to go beyond that in notebook-sized display panels. Many of the incremental improvements due from Sharp are materials-related and include better liquid crystals and improved retardation films—the coating that provide the phase shift needed for panel operation—play a key role in overall system performance.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Particle suspension
Glass
Glass
Transparent non-conductive coatings
Spacer and seal
Transparent electrically-conductive coatings
Light
Light
Particles in random positions (light is absorbed)
Particles aligned (light is transmitted)

6. Light-valve technology has many similarities with LCD technology but does not require the same level of complexity in manufacturing the devices. In light-valve technology, particles sandwiched between two glass panels align themselves when electric fields are present so that light can pass. Work is proceeding at Research Frontiers to find the suspended-particle materials that best fit the requirements of flat-panel displays.

In monochrome panels, Sharp will soon unveil improvements in five key features: contrast, response time, brightness, uniformity, and shadowing. The features depend on each other and in the past have involved making trade-offs between each other. Sharp is expected to improve all five features across the board, according to Pollack. Contrast will rise to 20:1 largely because of improvements in the retardation film, liquid-crystal material, and the conductive layers between the plates. Response time will be improved by making a thinner cell gap so a stronger field can be achieved for a given voltage. Display brightness will nearly double and begin to approach the brightness of CRTs because of improvements in the cold-cathode backlighting system. The combination of all the materials and system improvements will also yield a thinner panel—down from 7 mm in present technology to 5.5 mm next year.

ACTIVE-MATRIX COLOR

Perhaps in response to Motif's active-addressing technology innovation, Sharp's passive-matrix color panels will undergo a four-feature improvement. In color displays that use passive addressing, Sharp will move to a dual-scan technology that addresses a 480-row display as though it were two 240-row displays. Each row would be scanned twice as often as in conventional passive-addressing technology, which will result in higher contrast, faster response, better uniformity, and less shadowing. Color filters have been improved, particularly in red and blue saturation levels. Future products will provide color closer to active-matrix displays, which already exceed CRTs in color saturation performance, says Pollack.

Improvements are also in store for Sharp's active-matrix color displays. These include reduced power, higher information density, and larger panels. A 10.4-in.-diagonal display that once required 13 W will soon require just 7 W, explains Pollack, and the long-term goal is to reduce the power requirement to 3.5 W, which is equivalent to passive-matrix products. Dot pitch on monochrome active-matrix displays has been lowered to 0.18 mm (dot pitch is the distance from the center of one pixel to the center of the next). A 0.18-mm dot pitch is sufficient for a 1024-by-768-pixel resolution on a 11.8-in. display. It provides a line density of about 140 lines/in. The dot pitch in color displays is the distance between the pixels of the same color.

Displays are also getting larger. A 17-in.-diagonal AMLCD panel was demonstrated last year and Sharp will have a technology demonstration of a 20-in.-diagonal panel this year. Other innovations from Sharp include a process that will allow plastic to replace glass as the display substrate. This will create a much-lighter and more mechanically robust display. A 740-by-480-pixel prototype has already been fabricated. The idea, however, is not to make a less-expensive display. Plastic displays will, in fact, be more expensive than glass, at least initially. One primary market driver will be personal digital assistants (PDAs). In a mobile environment, displays must be rugged, and digitizing panels are preferred over keyboards as input devices.

Sharp and others continue to work on inherent LCD problems, such as a narrow viewing angle. Thinner cell gaps and a better compensation film—the layer that depolarizes the emitted light—are being developed. A ±20° viewing angle is sufficient for notebook computers, and that has been attained, says Pollack. He adds that viewing angles

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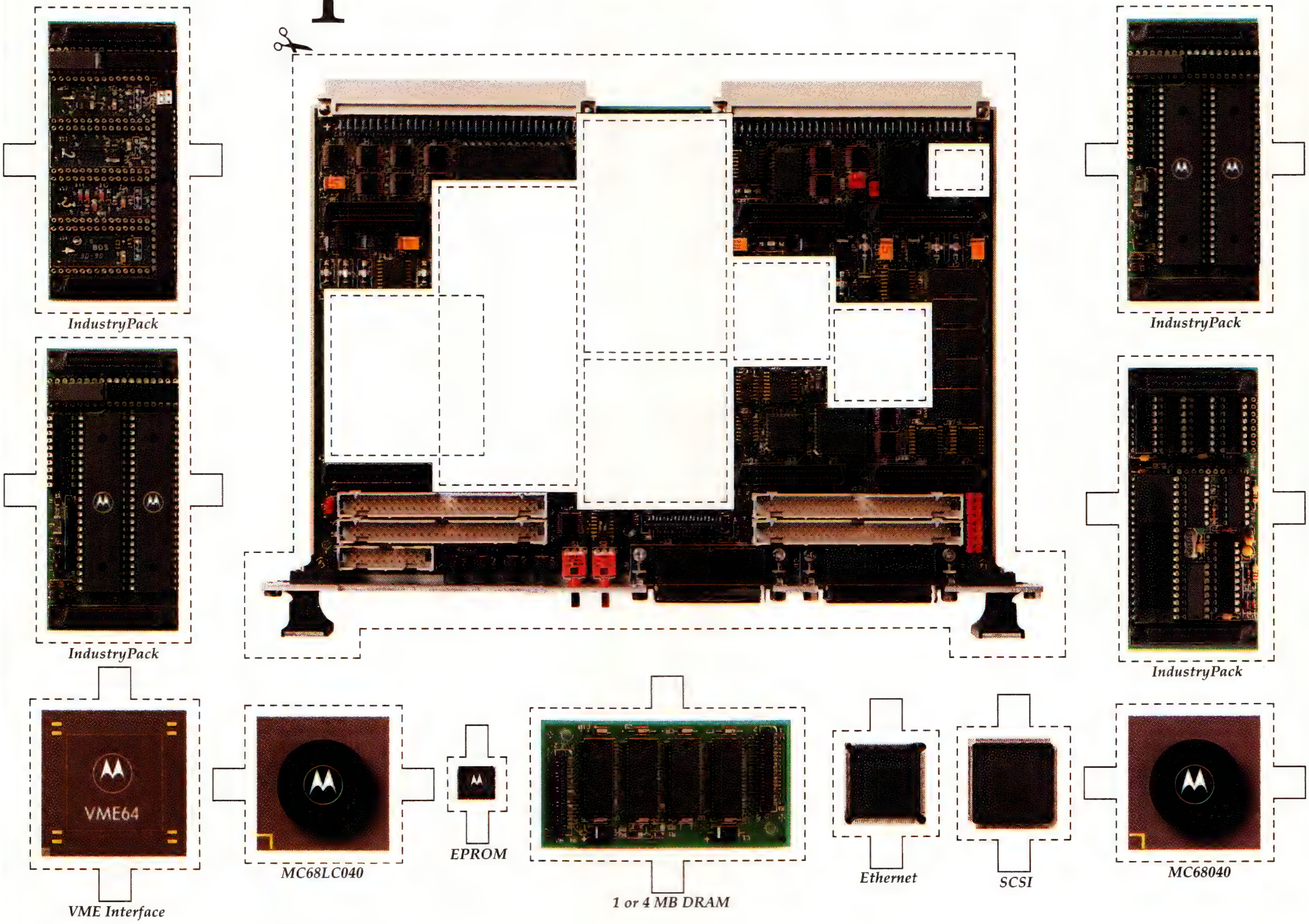

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of ±45° are possible. Even the bugaboo of AMLCDs, low yields, may be addressed by new technologies. At the International Solid States Circuits Conference in February, NEC Corp. and GTC Inc., both of Tokyo, Japan, described an error-compensation circuit that provides a five-fold improvement in yield without degrading system performance (ELECTRONIC DESIGN, *Mar. 4, p. 30).*

POLYSILICON TRIES HARDER

In the U.S., meanwhile, researchers at Xerox PARC continue to make strides in amorphous silicon flat-panel displays and push the technology envelope in the field of polysilicon. A 13-in.-diagonal AMLCD using amorphous silicon that integrates 6.3 million pixels will be demonstrated at the upcoming SID conference, says Malcolm Thompson, director of Xerox PARC's electronics and imaging laboratory. "We're running the amorphous silicon for the display in a routine process," he says. "It's highly documented and the idea is to use the most-difficult display we can produce to prove that we have a robust process."

In the polysilicon arena, Xerox is already supplying Hughes Aerospace with a 340-by-340-mm product that's processed at a temperature of 600°C. Eight months ago, Xerox announced the first thin-film-transistor fabrication on a substrate that large. Polysilicon requires a much higher temperature for deposition on the glass substrate, creating several technology challenges. The glass will actually shrink as a result of the heat, which means that subsequent lithography steps require a change in the image's magnification. This can, however, be corrected using a step-and-repeat lithography system (stepper) from MRS Technology Inc., Chelmsford, Mass. Xerox has successfully fabricated polysilicon devices on the panels, with the most complex to-date being a 6-bit DAC that runs at 20 MHz, says Thompson. The 20-MHz clock rate is sufficient for 2000-row displays, he says. Xerox also believes it can achieve 8-bit accuracy in its DACs to produce 8 bits of gray scale. In addition, Xerox has designed a universal controller that handles any arrangement of pixels—stripes, quads or triangles—and can compensate for temperature-initiated changes in liquid-crystal response. In addition, the chip will implement dithering and antialiasing techniques for better graphics performance (it eliminates "jaggies"). These techniques can be varied in different segments of the screen, says Thompson. This would be particularly useful in multimedia applications where one part of the screen displays graphics and another displays video. The chip, which Thompson describes as "quite large," is fabricated in 0.8-μm CMOS.

In large-scale, direct-view systems such as HDTV displays, liquid-crystal-based technologies will be getting tough competition from plasma displays. At next month's SID conference, Photonics Imaging Inc., Northwood, Ohio, will describe the technical details of a full-color, 30-in.-diagonal display. It will deliver higher spatial resolution than any other large, direct-view, color, emissive, flat-panel display previously demonstrated, says Peter Friedman, president and technical director. Prototypes of the display have been shown to the Defense Advanced Research Projects Agency *(Fig. 5).*

Although the technical details are still under wraps, Friedman said the 30-in. display successfully upscales the company's full-color 19-in. display unveiled last May. The 19-in. monitor achieves a spatial resolution of 42.6 pixels/in. for a full-color (RGB) pixel triad. Its 640-by-480-pixel matrix is progressively scanned at 60 frames/s. Line frequencies as high as 72 kHz—the scan rate of a workstation—have been achieved. Color is provided by exciting photophosphors with light from a xenon gas discharge. Color variation is implemented by 6 bits of gray-scale resolution for each red, green, or blue subpixel, which results in 262,144 colors. Production yields are eventually expected to reach 90%. The basic plasma technology used by Photonics is a double-substrate, two-electrode ac plasma-display panel (AC-PDP). The panel offers two primary advantages over conventional LCD technology. It's easier to implement a flicker-free picture, and it has a much wider viewing angle. In plasma displays, each pixel stays on until it's turned off, so it maintains the same brightness in spite of display size or resolution.

Technologies like LCDs that require scanning and refreshing to keep the pixel turned on experience a loss of brightness as display size or resolution grows, because each pixel is refreshed less frequently. Plasma displays implement cell memory by using a thick-film current-limiting capacitor at each cell site. The viewing angle of such displays is 160° because light is emitted from a 3D phosphor structure and is viewed directly. LCD technology, on the other hand, has an inherent requirement that the light be polarized. This means that at different viewing angles, light takes a slightly different path to the eye and can fall out of phase with the polarizer and lose contrast.

Plasma displays began to deliver color two years ago. Initially, researchers tried to produce color by using cells with different gases that glow with different primary colors, but that proved impractical. Now the technology of choice is to use a xenon-gas mixture that produces ultraviolet light when excited. This radiation excites a red, green, or blue phosphor applied inside the surface of each plasma cell. Each pixel consumes about 100 μW, and panel lifetimes appear to be on the order of 10,000 hours, says Friedman.

Color saturations for plasma displays are close enough to CRT performance to require either a video expert or a photometer to tell the difference. Friedman is optimistic that color plasma displays will surpass CRT color saturation. The photoluminescent phosphors (in which the phosphor is excited by photons) used in plasma displays haven't received nearly the research attention of cathoLuminescent phosphors (in which the phosphor is excited by electron bombardment) in CRTs, he says.

The 10,000-hour lifetime of plasma displays should also approach the 20,000-hour rated life of CRTs as research continues. A 60-in.-diagonal monochrome plasma display already in Photonics' product lineup, for example, has a rated lifetime of 50,000 hours. The number of colors in the 19-in. color model is presently 262,144 and represents the number of combinations that six bits of gray scale produce for each subpixel (red, green, and blue) that make up the pixel. Six bits isn't an inherent limitation of plasma but rather a limitation of the integration level of the electronics required for the column and row drivers. Photonics has designed an ASIC that will provide 8-bit color depth for each subpixel, which will result in a palette of 16 million colors, says Friedman. Besides delivering better color performance, the chip will eliminate a circuit board from the system. This will result in significant size and power savings.

Advances are also being made in electroluminescent (EL) displays. EL technology has taken some time to provide full-color displays worthy of integrating into notebook computers, but that's about to change, says James Hurd, president of Planar Systems Inc., Beaverton, Ore. Last year, Planar unveiled a multicolor display technology that uses red and green but not blue filters. It's manufactured using a proprietary inverted structure. Screen resolution is 640 by 350 pixels with a gray-scale level of 3 bits for each subpixel, and the refresh rate is 80 Hz. The EL display continues to have relatively high power demands, however, and the prototype consumes about 20 W. The display's structure is referred to as inverted because the panel isn't viewed through the substrate. Red and green color filters comprise the top layers and the light is produced by a yellow phosphor. Significant progress has been made in creating compounds that emit blue light that's bright enough to meet standards requirements, says Hurd, and Planar has reported ternary compounds reaching the 3.6-fL requirement of the ANSI/HFS-100 standard. This year, Planar will have a technology demonstration of a full-color display in which the panel is viewed through the substrate. The display will have 640-by-480-pixel resolution and use a tape-automated-bonding (TAB) interconnect technique to achieve a color-dot pitch (red, green, and blue pixels) of just 330 μm, explains Hurd. A full-color pilot line is expected to be completed in the third quarter of this year with product following in 1994.

DARK-HORSE TECHNOLOGIES

A recurring theme in the recent history of flat-panel-display technology is that new technologies are always being developed to challenge the complex and sophisticated products based on liquid-crystal materials. One of the most innovative dark horses, which has not yet reached the level of development as Kopin's Smart Slide, or even the FED technologies, is the light-valve display.

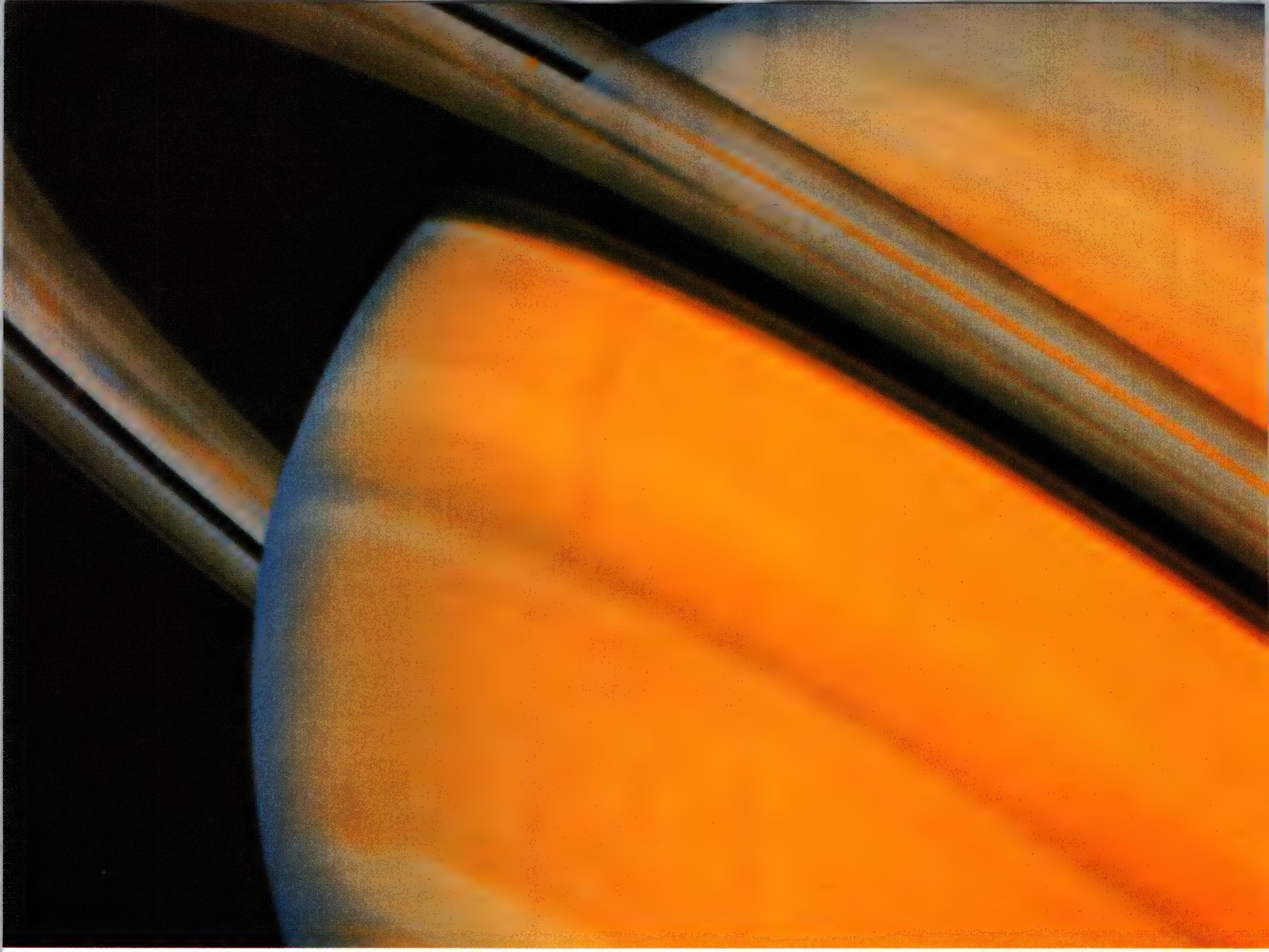
Light-valve technology is based upon the effect of an electric field on polarizing materials in liquid suspension. Suspended-particle displays (SPDs) consist of a cell comprised of transparent walls, with patterned electrodes on the inside surface of each cell wall. A thin dielectric overcoating covers each electrode. The cell is sealed after being filled with the liquid suspension, and electrical connections pass through the seal to an external ac voltage. With the voltage off, the suspended particles take random positions and the suspension is dark blue. When ac voltage is applied, the particles align and allow light to pass *(Fig. 6)*. "The construction of an SPD cell is similar to that of an LCD, but much simpler," says Robert Saxe, president of Research Frontiers Inc., Woodbury, N.Y., the leading proponent of SPD technology.

Unlike LCDs, SPDs don't require sheet polarizers, which leads to several superior performance characteristics. Contrast ratio and brightness involve a trade-off. SPDs can deliver contrast ratios of 1000:1 with light transmission of 0.01% to 10%, or, light transmission of 44% with a contrast ratio of 11:1, to cite two examples. The trade-off can be tailored to the application by changing the concentration of particles in the SPD. In addition, viewing angle is superior to LCDs. At 30°, for example, about 50% of the total light transmitted through the panel can reach the viewer's eye.

But for all of its potential, SPD technology is still in its early stages of development. Work continues on materials such as polyiodides to speed response time, which is now around 100 ms, says Saxe. Proprietary polymers appear to offer even better speed performance and address the problem of agglomeration: the tendency of particles to stick together and form lines on the display screen. Still another materials development, a film form of fluid suspensions, has been announced, but Saxe is disclosing little about the technology.

The intensity of the research effort in flat-panel-display technologies make it clear that the industry will grow even faster in the future. New markets such as handheld computers, video games, and virtual-reality applications call for new, or at least vastly improved, technologies. For the designer of these systems, the choice of a flat-panel display will become more challenging. Only by monitoring the entire range of choices can the best product of the future be designed.☐

HOW VALUABLE?	CIRCLE
HIGHLY	590
MODERATELY	591
SLIGHTLY	592



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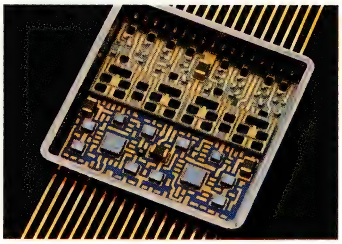

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INCREASE SYSTEM THROUGHPUT BY COMBINING SCSI BUS MASTERING WITH LOCAL DEDICATED MEMORY TO MAXIMIZE DATA-TRANSFER RATES.

In this age of ever-expanding information, streamlining the flow of information from one point to another is critical. Advances in hardware and software demand that high-end PCs and workstations transfer data at rates previously unheard of. For this reason, SCSI interfaces and host adapters must be constantly enhanced to provide increased performance and bandwidth for these high-performance systems. By adding local memory and intelligence to a bus-mastering SCSI host adapter, designers can create high-performance solutions to meet the demanding data-transfer requirements of today's and tomorrow's high-end systems.

SCSI interfaces are often categorized by the method used to transfer data from the SCSI bus to the final destination in host memory. Using such an approach, SCSI host adapters fall into one of three categories: CPU assisted, DMA slave, or bus master.

Each succeeding category increases performance by reducing hardware and software overhead to the host system. However, the increased performance has a cost associated with it because increasing intelligence must be embedded in the SCSI host adapter or subsystem. The designer must determine the price/performance benefits and trade-offs of each alternative.

Of the three classes, the bus-master approach provides the highest performance. They're typically targeted for high-end PCs and workstations and can take advantage of such high-performance buses as EISA, Micro Channel, SBus, and so on. Because it has its own embedded processor and DMA controller, a bus-mastering SCSI adapter or subsystem can fetch its own instructions. Furthermore, it can initiate its own data transfers across the host bus without any assistance from the CPU or DMA controller. This reduces CPU and SCSI protocol overhead, while at the same time increasing raw data-transfer rates and system-level efficiency.

To take SCSI bus mastering one step further, if the SCSI adapter doesn't have to access the host bus to fetch instructions or transfer data, it could further improve its transfer efficiency. Data can be temporarily stored in some type of dedicated memory, then transferred to system memory using high-speed, large burst transfers over a high-speed bus. By placing dedicated pro-

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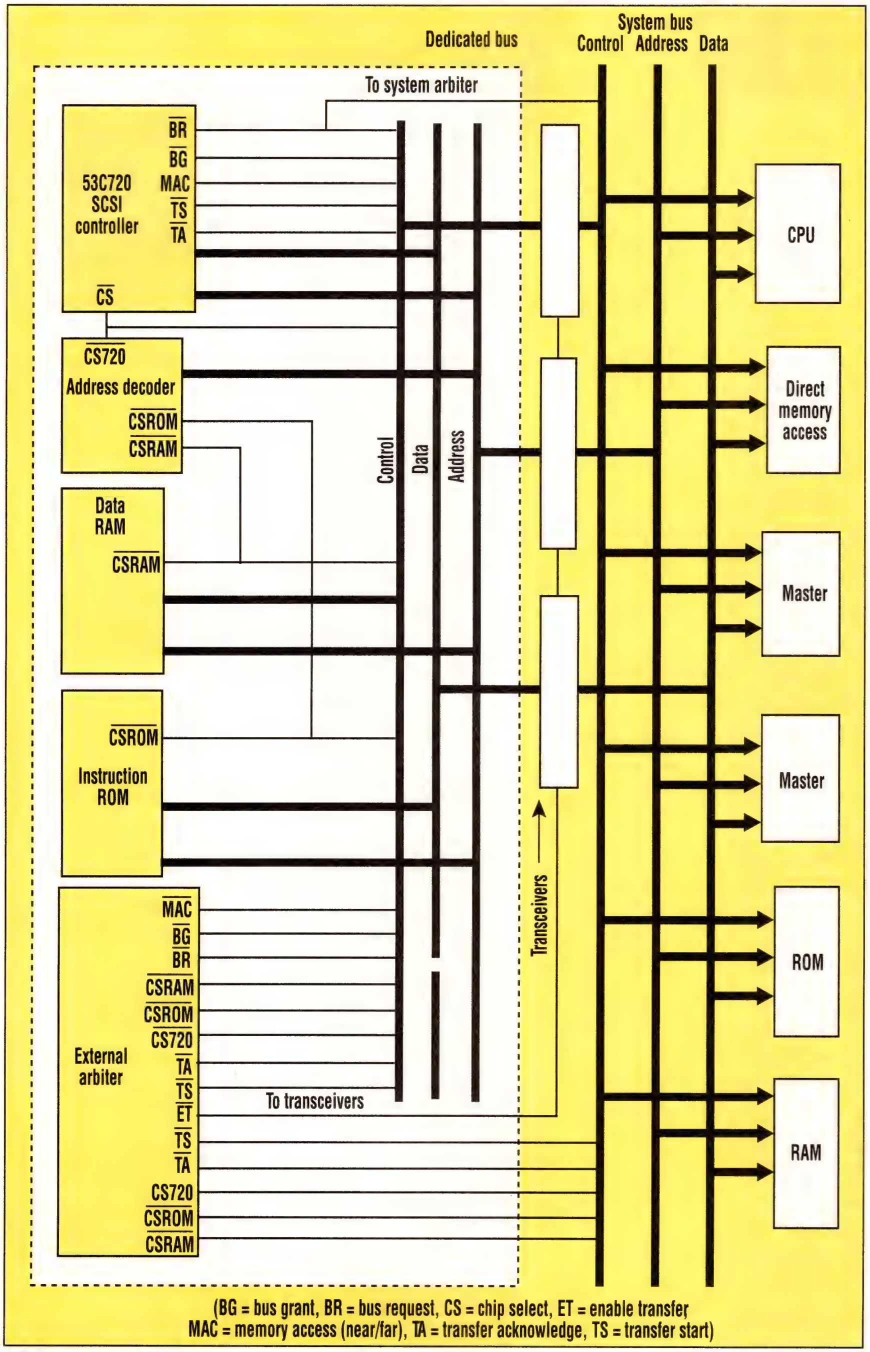
NCR Corp., 1635 Aeroplaza Dr., Colorado Springs, CO 80916; (719) 596-5795.

gram memory (ROM, PROM, EPROM) and data memory (RAM) on a private or dedicated bus, design engineers can essentially isolate the SCSI bus master from the system bus. This isolation not only increases I/O transfer performance, but also decreases the overall system latency because there's less demand placed on the host bus.

By definition, a bus master owns the bus and is responsible for driving the address, data, and control lines. CPU-controlled and DMA-slave adapters require a microprocessor, a DMA controller, and a SCSI controller to implement the SCSI protocol from the host side. In the CPU-controlled adapter, the microprocessor acts as the bus master by fetching instruction sequences as needed and feeding them to the SCSI controller to perform the requested operation. The embedded CPU then directs the DMA controller to initiate the transfer of data across the host bus via the SCSI controller. In the case of a DMA-slave adapter, the DMA controller acts as the bus master and initiates the transfer of data to and from SCSI peripherals across the host bus.



1. BY ADDING DEDICATED LOCAL MEMORY and a bus arbiter to the SCSI subsystem (area in dashed box), bus activity on the main system bus can be reduced. This lowers the overhead operations required by the host processor. The dedicated-local-memory bus in the SCSI subsystem allows the 53C720 to do many operations without interrupting the host system.

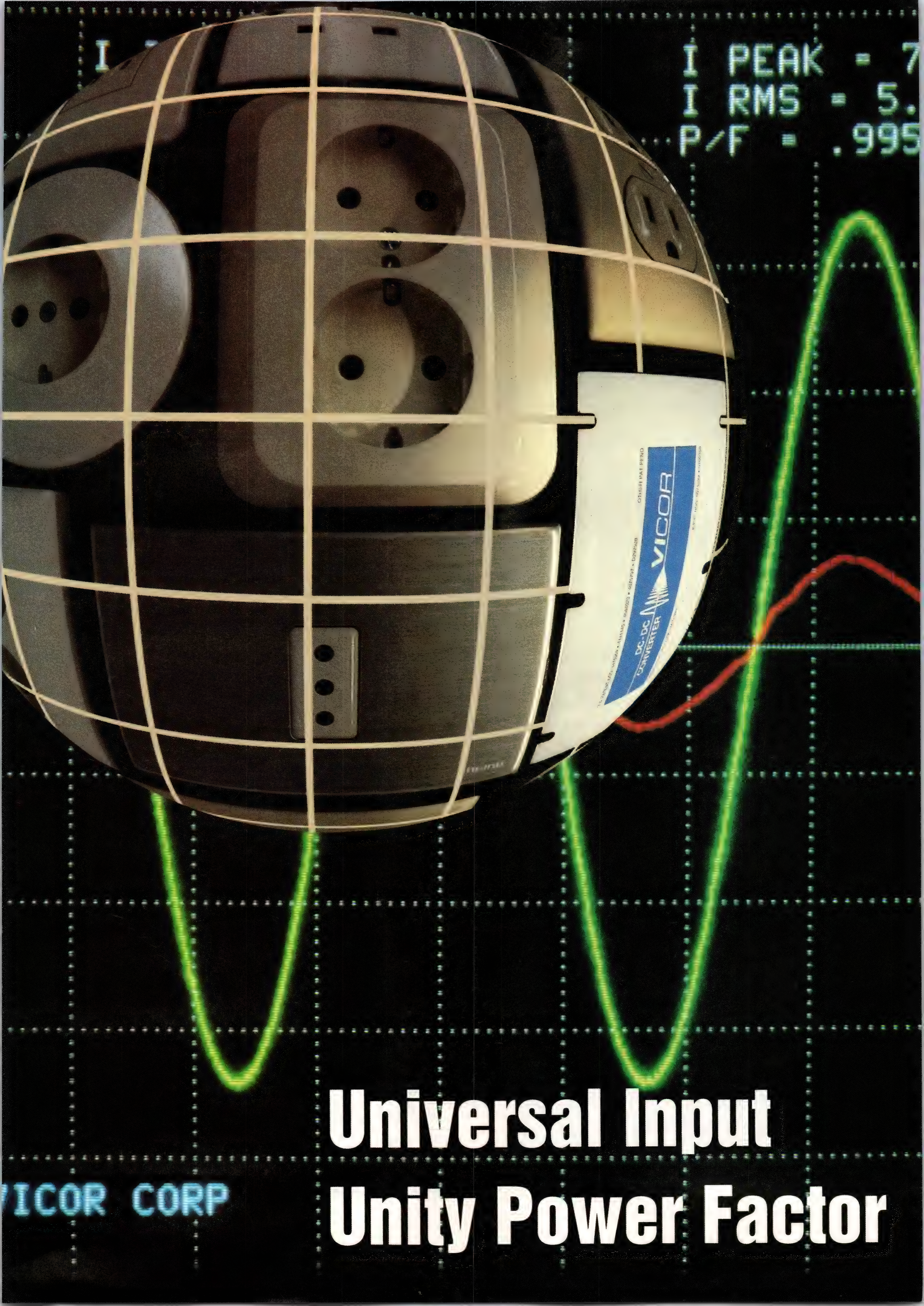
Like the host CPU and other bus-master devices, a SCSI bus-master adapter can bypass the DMA controller and become the bus master by arbitrating for the system bus. Once the SCSI adapter is acknowledged by the system arbiter that it has the bus, it begins performing zero-wait-state bus cycles. Thus, the bus-master approach offers a significant performance advantage over other SCSI adapter solutions.

If a DMA-slave adapter is used, the DMA-slave bus cycle is usually much longer than required because the DMA controller has to verify that the SCSI adapter recognizes a Data Acknowledge (DACK) signal and gates its data onto the bus. Consequently, the DMA controller inserts one or two wait states to lengthen the bus cycle, then uses an extra cycle for a read/write sequence. Furthermore, the DMA-slave adapter typically employs only a 16-bit-wide host interface.

A bus-master SCSI adapter must have SCSI, DMA, and high-level language capabilities to provide the performance required by today's high-speed buses. By directly executing high-level language instructions rather than interpreting instructions from a CPU, a SCSI bus master reduces SCSI overhead and increases system performance.

An example of such a bus-master chip is NCR's 53C720 SCSI I/O processor. With a SCSI core, DMA core, and SCRIPTS processor (NCR's high-level language execution unit), the 53C720 reduces SCSI I/O start latency to 500 ns, compared to the 2-8 ms that most other intelligent SCSI solutions require.

In its basic configuration, the 53C720 can be used as a SCSI bus-



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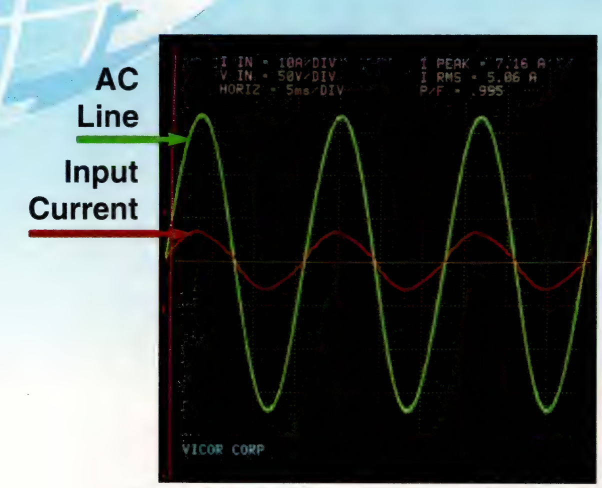

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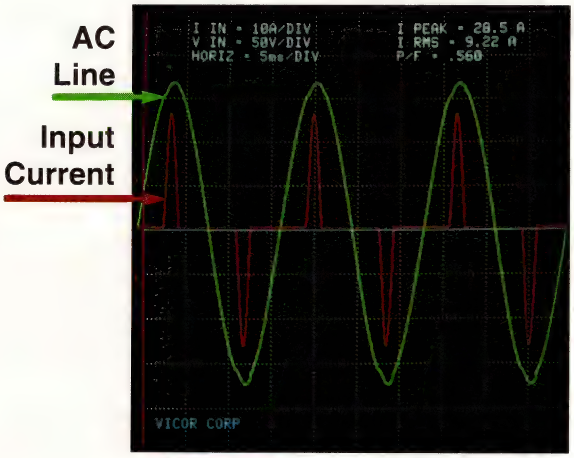

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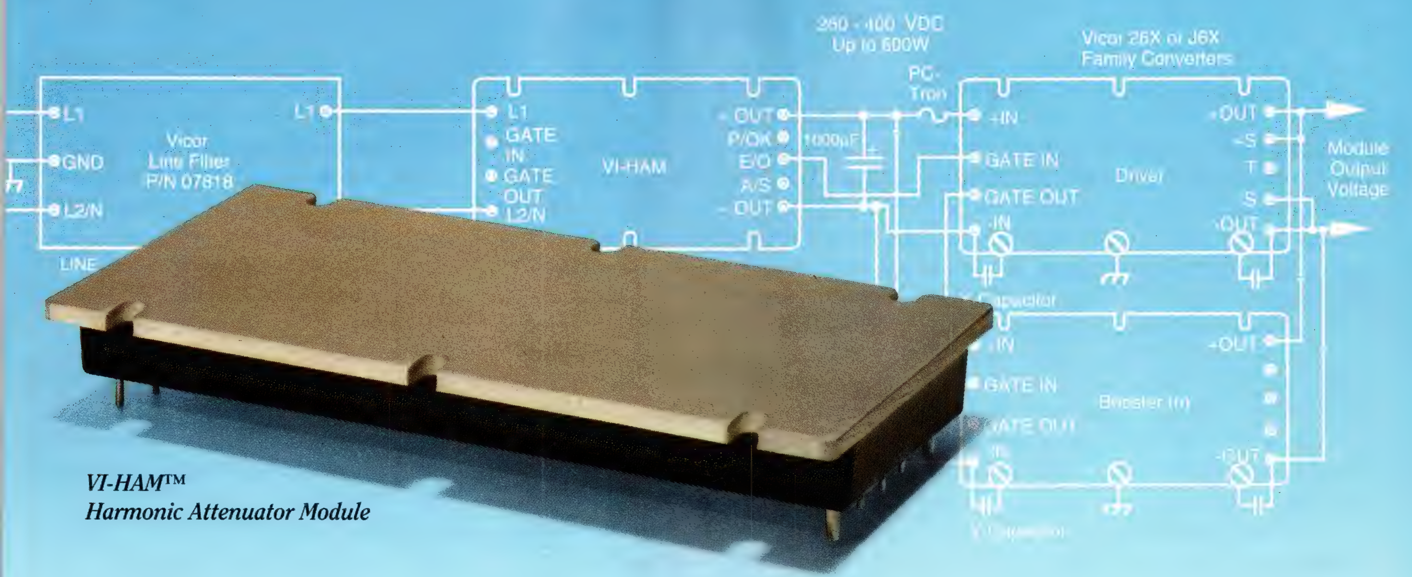

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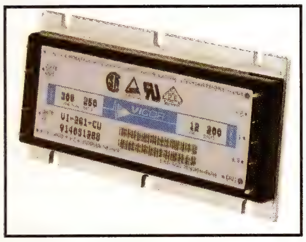

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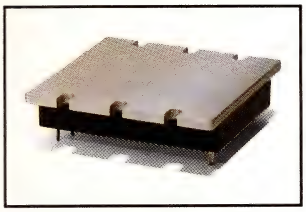

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master adapter with a CPU direct interface *(Fig. 1)*. The chip can serve as a SCSI bus master in systems that support the Motorola 68030, 68040, and Intel's 80X86 processors. With some glue logic, the bus master can tie into high-performance processors, such as the 80486 and the 80960.

To accompany the embedded CPU and DMA controller on the SCSI chip, a typical host adapter circuit design would require just some ROM, RAM, a bus arbiter, and some bus transceivers for a dedicated 32-bit bus interface.

The rest of the system might typically contain several other bus master devices, a host CPU, DMA channel control logic and more RAM and ROM *(Fig. 1, again)*. The large area in dashed lines represents a dedicated memory design.

Let's first examine how a SCSI I/O processor functions as a bus master on the host system bus and how it functions on a dedicated bus, then compare the essential performance differences (gains) between the two. The three functional blocks of the SCSI processor (SCSI controller, embedded RISC CPU, and DMA controller) work together to provide a SCSI bus-master solution. Unlike previous generation devices, the SCSI core can be controlled by the integrated DMA core through a high-level logical interface.

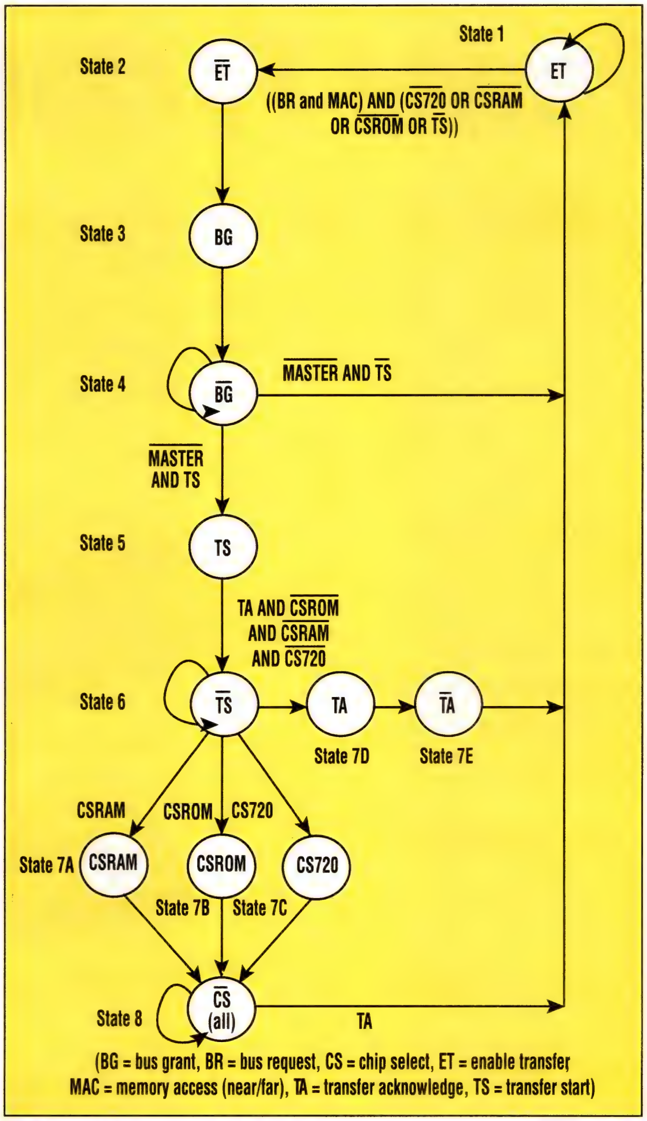
Commands, each 64 bits wide, control the SCSI core (the instructions are fetched from the main host memory). They instruct the core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information/Data, Change Bus Phases, and in general, implement all aspects of the SCSI protocol. In fact, there's a one-to-one correlation between a SCSI SCRIPT and SCSI protocol, so that any SCSI situation can be handled by a SCRIPT.

The DMA core acts as the bus-master DMA device. It supports either 16- or 32-bit memory transfers and automatically supports misaligned DMA transfers. Having a 64-byte FIFO on the chip allows the SCSI I/O processor to burst 2, 4, 8, or 16 long words across the memory bus interface.

The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor. The SCSI SCRIPTS processor allows SCSI and memory-to-memory move instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTS are typically executed from 16- or 32-bit system memory. Because a SCSI SCRIPT is executed independently of the host CPU and system bus in use, both I/O and system performance are significantly enhanced.

Turning the SCSI subsystem into a bus master is a fairly straightforward process. First, the host CPU writes the starting address of the SCRIPT to the Data SCRIPTS Pointer (DSP) register (if using dedicated memory, $\overline{\text{AUTO}}$ is asserted and the SCRIPT is automatically fetched from location zero). The SCSI I/O processor begins the bus master process by asserting a Bus Request (BR) onto the system bus. The 53C720 then waits for the Bus Grant (BG) response from the system arbiter. Once the SCSI I/O processor is granted, the bus will deassert BR. The SCSI processor checks that Bus Busy (BB) is deasserted and then asserts its BB and Master signals to gain control of the bus for a data transfer.

Bottlenecks on the bus, however, can limit the performance of the standard bus-master SCSI controller. By placing the controller on a dedicated bus with its own local memory, a bus-master SCSI subsystem can deliver its highest performance. When the SCSI adapter has access to dedicated ROM and RAM, the traffic on the host bus resulting from an I/O operation is minimized to a single interrupt.


State 1
ET
State 2
$\overline{\text{ET}}$
((BR and MAC) AND ($\overline{\text{CS720}}$ OR $\overline{\text{CSRAM}}$
OR $\overline{\text{CSROM}}$ OR $\overline{\text{TS}}$))
State 3
BG
State 4
$\overline{\text{BG}}$
$\overline{\text{MASTER}}$ AND $\overline{\text{TS}}$
$\overline{\text{MASTER}}$
AND TS
State 5
TS
TA AND $\overline{\text{CSROM}}$
AND $\overline{\text{CSRAM}}$
AND $\overline{\text{CS720}}$
State 6
$\overline{\text{TS}}$
TA
$\overline{\text{TA}}$
State 7D
State 7E
CSRAM
CSROM
CS720
State 7A
CSRAM
CSROM
CS720
State 7B
State 7C
State 8
$\overline{\text{CS}}$ (all)
TA
(BG = bus grant, BR = bus request, CS = chip select, ET = enable transfer
MAC = memory access (near/far), TA = transfer acknowledge, TS = transfer start)

2. THE BUS ARBITER required by the SCSI subsystem can be implemented in programmable logic. The eight basic states and straightforward control sequences make it easy to convert the state diagram into programming terms for the PLD.

There are several benefits to using dedicated memory. First, bus latency decreases because there's less arbitration for the host bus, increasing system performance. Host bus traffic also decreases because the SCSI controller now has dedicated access to SCRIPTS instructions and doesn't have to access program memory over the host bus. Finally, I/O performance increases by using dedicated RAM to store the data. That data is then transferred to main memory in larger blocks using faster rates (in the same bus ownership period).

An example of decreased

latency and increased performance can be worked through using the Extended Industry Standard Architecture (EISA) bus *(Table 1)*. In the example, assume there are two DMA channels, one block, one single cycle, and an 8-MHz bus clock. With two bus masters, the bus-master-grant latency could be as high as 46.3 µs. With six bus masters, this potential latency increases to 173.5 µs, which means that the SCSI adapter could transfer for 10.6 µs before it relinquishes the bus. But the adapter may then wait for another 173.5 µs before continuing the transfer.

These numbers are most definitely worst-case latencies, and don't reflect a typical system. Throughout the remainder of this article, worst-case numbers are used for the purpose of comparison only. They shouldn't be confused with more realistic actual design latencies.

MEMORY COMPARISONS

Now let's consider the performance of single-threaded and multi-threaded read operations using system memory (far memory) vs. dedicated memory (near memory).

In the past, single-threaded applications using system memory adequately supported the number of I/O devices and performance levels required by users. A SCRIPT for a single-threaded initiator read selects a target device, then reads a 512-byte block of data from the target device and moves it to an address in either dedicated or far memory. This application is common because data on a disk drive usually resides in 512-byte blocks.

The SCSI adapter may place the data in small, manageable pages in main memory, supporting virtual-memory schemes. Performance can be measured by comparing the number of arbitrations and the number of clocks required for instruction fetches and data transfers when reading 512 bytes, 2048 bytes, and 1 Mbyte from a SCSI device, then placing the data in either dedicated memory or far memory *(Table 2a)*.

Far memory is accessed via the EISA bus running at 8 MHz with two bus masters accessing the bus. It's important to remember that this read typically requires only one interrupt from the CPU upon completion of the data transfer.

Most SCSI adapters would require an interrupt for every 512-byte block—2048 interrupts for a 1-Mbyte transfer. Using dedicated memory, a 512-byte read uses 326 clock cycles, or 40 µs at 8 MHz. Of those cycles, 40% are used for instruction fetches, and the remaining 60% are used for data transfers. When reading 1 Mbyte, 48 ms are required for the transfer—6% for fetches and 94% for data transfer.

Now compare this same read operation using the system bus and far memory instead of dedicated memory. The 512-byte read could use up to 1.6 ms, or 40 times more than dedicated memory requires. The 1-Mbyte read could take up to almost 1 second—20 times more time than used by dedicated memory. The percentage between fetches and data transfers remains about the same for either dedicated or far memory.

A multi-threaded environment is becoming more popular as high-performance PCs and workstations use more and more peripheral devices. For example, a single high-end system could typically include a printer, tape drive, disk drive, optical disk, CD-ROM, etc. If a slower device is being accessed, such as a printer, a multi-threaded application allows other devices to be accessed in parallel. With earlier generations of SCSI adapters, it would take thousands of lines of code to generate this type of application. But with the introduction of SCRIPTS and other high-level languages, multi-threading becomes second nature.

In much the same manner as the single-threaded read SCRIPT, the multi-threaded SCRIPT selects a target device, then reads 512-byte blocks of data from the target device and moves the data to an address in either dedicated or far memory. The number of arbitrations and number of clocks required for instruction fetches and data transfers can readily be compared to the single-threaded operations previously described *(Table 2b)*. Again, when using these numbers for comparison purposes, remember to factor in the number of system interrupts required by the SCSI adapters being used.

To perform a 512-byte read using dedicated memory, 516 clocks are required. When far memory is used, as much as 3 ms may be required. The percentage of clocks required for opcode fetches versus data transfers is

TABLE 1: EISA BUS LATENCY CALCULATIONS

Bus Grant Sequence:	2 Bus Masters	6 Bus Masters
DMA channel 1	5.0	5.0
Refresh	1.3	1.3
CPU	9.0	9.0
DMA channel 2	1.1	1.1
Bus master 1	10.6	10.6
DMA channel 1	5.0	5.0
Refresh	1.3	1.3
CPU	9.0	9.0
DMA channel 2	1.1	1.1
Refresh	1.3	1.3
Bus master 2	Grant	10.6
DMA channel 1	na	5.0
Refresh	na	1.3
CPU	na	9.0
DMA channel 2	na	1.1
Refresh	na	1.3
Bus master 3	na	10.6
DMA channel 1	na	5.0
Refresh	na	1.3
CPU	na	9.0
DMA channel 2	na	1.1
Refresh	na	1.3
Bus master 4	na	10.6
DMA channel 1	na	5.0
Refresh	na	1.3
CPU	na	9.0
DMA channel 2	na	1.1
Refresh	na	1.3
Bus master 5	na	10.6
DMA channel 1	na	5.0
Refresh	na	1.3
CPU	na	9.0
DMA channel 2	na	1.1
Refresh	na	1.3
Bus master 6	na	Grant
Bus master grant latency	46.3	173.5

Assumptions: 2 DMA channels—1 block; 1 single-cycle 8-MHz clock; All times are in microseconds

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significantly greater in a multithreaded environment due to the required extra code. Yet when transferring larger blocks of data, say 1 Mbyte, the percentage is essentially equal. Again, 48 ms are needed for a 1-Mbyte transfer using dedicated memory, while up to 1 second is required when far memory is used and worst-case system-bus latencies occur. Again, this excludes any other interrupts that could be generated by the CPU.

The number of arbitrations for instruction fetches significantly decreases if a larger block size is used to transfer the data. In Tables 2a and 2b, a 512-byte block is used for all of the examples.

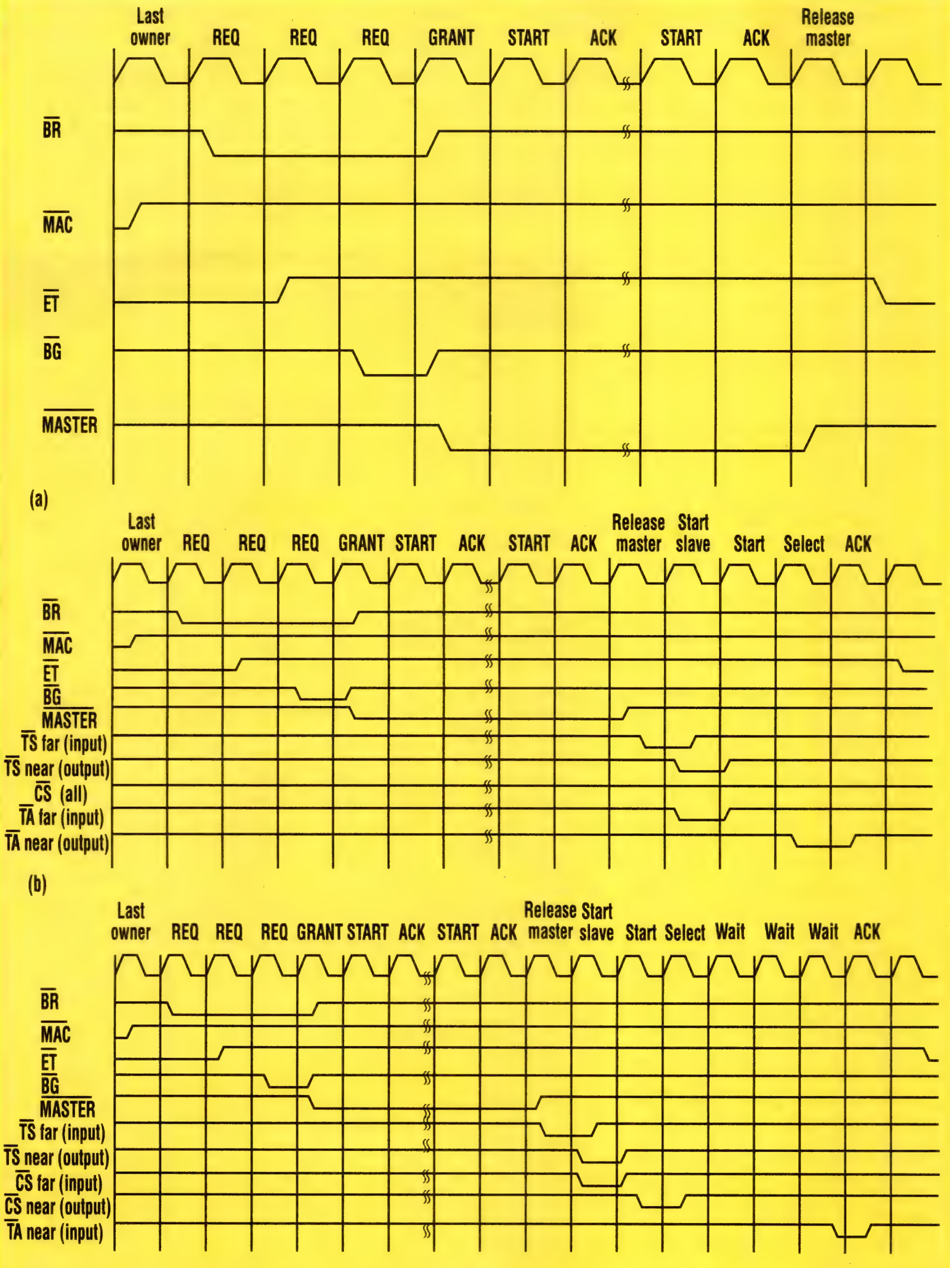
If a 2-kbyte block size is employed, only one move instruction is required to transfer 2048 bytes, while 512 move instructions (versus 2048 for the 512-byte block) are needed to transfer 1 Mbyte of data. If a 1-Mbyte block is used to transfer data, the number of arbitrations goes from 2048 to 1 for each move instruction. That would reduce the number of clocks to 12 instead of 24,576. Such a change would mean that over 99% of the clocks would now be used for actual data transfer, thus reducing overhead time.

Table 2b also indicates when it's best to use dedicated ROM, RAM, or both. When transferring a 512-byte block, 60% of the clocks perform the instruction fetch. If these instructions were located in dedicated ROM or PROM, the SCSI I/O processor would not have to arbitrate for the system bus before executing the instruction. Because only 40% of the clocks transfer the data, system RAM could be used in this instance.

When 1 Mbyte is transferred, only 6% of the clocks are used for instructions, while the remaining 94% are involved with data transfer. In this case, it would be imperative to have dedicated RAM. Once data is stored in dedicated RAM, a high-speed data bus can be used to transfer larger blocks of data to system memory at an extremely fast burst transfer rate. Due to the limitations of the EISA bus running at 8 MHz, data can be transferred for only 10.6 μs before the master must give up control of the bus for another arbitration cycle.

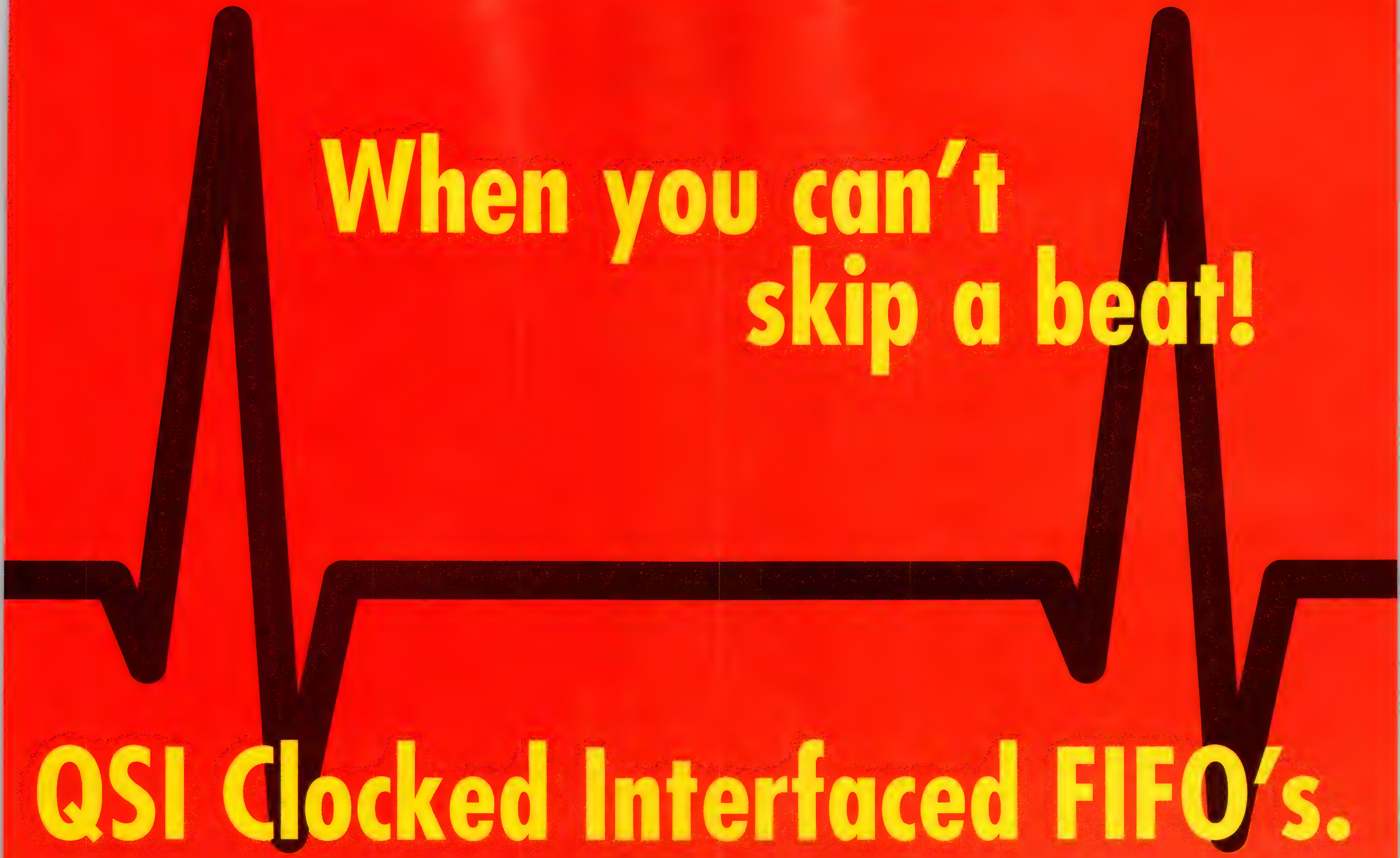
A key element of the SCSI subsystem design is the external arbiter that acts as a buffer between the system bus and the SCSI I/O processor. If the SCSI processor wants to access only dedicated memory, it still must arbitrate with the host bus to access only the dedicated bus. However, the external arbiter allows the SCSI processor to access the dedicated memory without delay.

The $\overline{\text{MAC}}$ signal (also referred to as the near/far pin), will be asserted high when the transfer is to dedicated memory. The pin will be tied to the external arbiter, and each time the SCSI processor is accessing itself or dedicated memory, the arbiter disables the transceivers



(ACK = acknowledge, BG = bus grant, BR = bus request, CS = chip select, ET = enable transfer, MAC = memory access (near/far), REQ = request, TA = transfer acknowledge, TS = transfer state

3. THE MASTER CYCLE on the bus can be divided into three types of activities: a cycle with no dedicated access (a), a cycle with host activity but no dedicated accesses (b), and a cycle with dedicated access (c).



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and stores any Transfer Start ($\overline{TS}$) and Chip Select ($\overline{CS720}$, $\overline{CSROM}$, or $\overline{CSRAM}$) signals from the system bus. The only time that a $\overline{TS}$ or $\overline{CS}$ will occur is during an interrupt or error condition.

Once the processor completes its dedicated access, the arbiter generates any necessary $\overline{TS}$ and $\overline{CS}$ signals, and enables the transceivers for normal operation. From the system bus perspective, the transfer will proceed as if wait states had been inserted into the cycle. The address is valid for an entire cycle.

The external arbiter can be implemented using a programmable logic device and code generated by a state-machine diagram that describes the operation *(Fig. 2)*.

Just eight basic states are needed to implement the state machine, as can be seen in the diagram. Those eight states and the conditions they require are as follows:

State 1: In state 1, four conditions can occur:

1) The CPU is the bus master and accesses far memory (SCSI processor, dedicated ROM or RAM);

2) The CPU is the bus master and accesses system memory;

3) The SCSI I/O processor is the bus master and accesses dedicated memory (SCSI processor, dedicated ROM or RAM);

4) The SCSI I/O processor is the bus master and accesses far memory (system memory).

If conditions 1, 2, or 4 occur, the external arbiter remains in state 1. If condition 3 occurs and the CPU isn't accessing the SCSI processor or dedicated ROM or RAM, the arbiter will disable the transceivers. Note: The SCSI processor requests the use of the system bus before a dedicated memory access. The system bus arbiter will grant the processor the system bus, but the processor uses the dedicated bus rather than the system bus. At this point, the two buses are entirely separated from each other. The external arbiter must be modified if the system arbiter is expecting a $\overline{TS}$ signal once a bus request occurs.

State 2: The transceivers are disabled and the dedicated bus is isolated from the system bus.

State 3: The jump to state 3 is taken during the next clock edge. A Bus Grant is generated by the external arbiter, which gives the SCSI processor access to the dedicated bus.

State 4: The jump to state 4 is taken on the following clock edge. The Bus Grant signal is deasserted and the SCSI processor remains in state 4 until the dedicated access is completed and the master is deasserted. While the processor is the bus master, the external arbiter latches any $\overline{TS}$ that occurs on the system bus. If a $\overline{TS}$ isn't latched, the arbiter jumps back to state 1 (see associated timing diagram in Figure 3a). If a $\overline{TS}$ is latched, the arbiter jumps to state 5.

State 5: The external arbiter regenerates a TS signal for the SCSI I/O processor.

State 6: The external arbiter deasserts $\overline{TS}$ for the SCSI I/O processor. The arbiter exits from this state if a Transfer Acknowledge (TA) on the system bus occurs and the slave access on the system bus isn't for the SCSI processor. The arbiter remains in this state until the slave cycle is completed by another slave device or until a $\overline{CS}$ for dedicated memory occurs. If a CSROM, CSRAM, or CS720 occurs, the arbiter exits this state and goes into state 7.

State 7A through 7C: The respective chip select is asserted.

State 7D: The external arbiter generates a TA because the $\overline{TS}$ was intended for some other slave device. The TA enables the SCSI processor to receive another $\overline{TS}$. The arbiter flows to state 1 during the next rising edge (see associated timing diagram in Figure 3b).

State 7E: The external arbiter deasserts TA and flows to state 1 during the next rising edge.

State 8: Chip Selects are deasserted. The arbiter remains in this final

TABLE 2A: LOCAL MEMORY VS. FAR MEMORY PERFORMANCE FOR SINGLE-THREADED READ

				Decicated Memory			Far Memory	
Block size	Instruction	# of Arb		Clks/ Arb		# of Clks	Lat/ Arb	# of Clks
512 bytes	SCRIPT FETCH	15	×	6	=	90	370.4	5631.0
	MOVE	1	×	6	=	6	370.4	375.4
	M to M MOVE							
	IND. FETCH	5	×	6	=	30	370.4	1877.0
	MOVE	1	×	6	=	6	370.4	375.4
	Total FETCH	22 (64.7%)				132 (40.5%)		8258.8 (64.1%)
	Data Transfer	12 (35.3%)				194 (59.5%)		4626.8 (35.9%)
	Total	34 (100%)				326 (100%)		12885.6 (100%)
2048 bytes	SCRIPT FETCH	15	×	6	=	90	370.4	5631
	MOVE	4	×	6	=	24	370.4	1501.6
	M to M MOVE							
	IND. FETCH	5	×	6	=	30	370.4	1877
	MOVE	4	×	6	=	24	370.4	1501.6
	Total FETCH	28 (43.8%)				168 (18.9%)		10511.2 (42.8%)
	Data Transfer	36 (56.2%)				722 (81.1%)		14056.4 (57.2%)
	Total	64 (100%)				890 (100%)		24567.6 (100%)
1 Mbyte	SCRIPT FETCH	15	×	6	=	90	370.4	5631.0
	MOVE	2048	×	6	=	12288	370.4	768819.2
	M to M MOVE							
	IND. FETCH	5	×	6	=	30	370.4	1877.0
	MOVE	2048	×	6	=	12288	370.4	768819.2
	Total FETCH	4116 (20.1%)				24696 (6.4%)		1545146.4 (19.4%)
	Data Transfer	16388 (79.9%)				360466 (93.6%)		6414193.2 (80.6%)
	Total	20504 (100%)				385162 (100%)		7959339.6 (100%)

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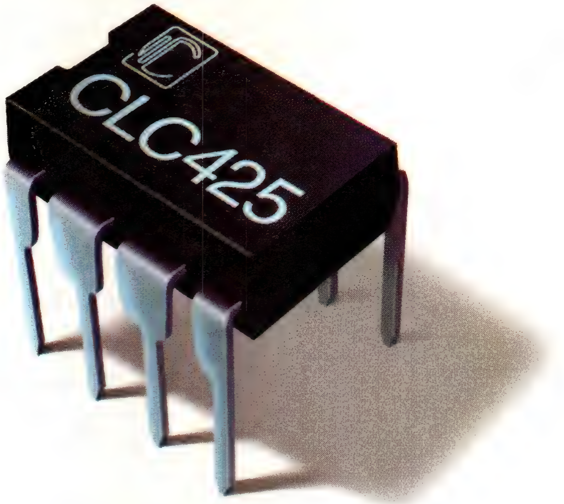

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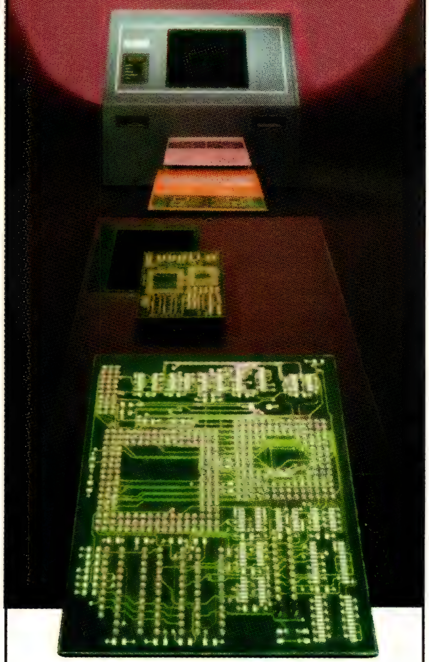
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TABLE 2B: LOCAL MEMORY VS. FAR MEMORY PERFORMANCE FOR MULTI-THREADED READ

				Local Memory			Far Memory	
Block size	Instruction	# of Arb		Clks/ Arb		# of Clks	Lat/ Arb	# of Clks
512 bytes	SCRIPT FETCH	39	×	6	=	234	370.4	14640.6
	MOVE	1	×	6	=	6	370.4	375.4
	M to M MOVE	2	×	8	=	6	370.4	754.8
	IND. FETCH	8	×	6	=	48	370.4	3003.2
	MOVE	1	×	6	=	6	370.4	375.4
	Total FETCH	51				310		19149.4
		(77.3%)				(60.1%)		(77.0%)
	Data Transfer	15				206		5747.0
		(22.7%)				(39.9%)		(23.1%)
	Total	66				516		24896.4
		(100%)				(100%)		(100%)
2048 bytes	SCRIPT FETCH	39	×	6	=	234	370.4	14640.6
	MOVE	4	×	6	=	24	370.4	1501.6
	M to M MOVE	2	×	8	=	16	370.4	754.8
	IND. FETCH	8	×	6	=	48	370.4	3003.2
	MOVE	4	×	6	=	24	370.4	1501.6
	Total FETCH	57				346		21401.8
		(61.3%)				(32.0%)		(60.4%)
	Data Transfer	36				734		14032.4
		(38.7%)				(68.0%)		(39.6%)
	Total	64				890		24567.6
		(100%)				(100%)		(100%)
1 Mbyte	SCRIPT FETCH	39	×	6	=	234	370.4	14640.6
	MOVE	2048	×	6	=	12288	370.4	768819.2
	M to M MOVE	2	×	8	=	16	370.4	754.8
	IND. FETCH	8	×	6	=	48	370.4	3003.2
	MOVE	2048	×	6	=	12288	370.4	768819.2
	Total FETCH	4145				24874		1556037.0
		(20.2%)				(6.5%)		(19.5%)
	Data Transfer	16388				360478		6414205.2
		(79.8%)				(93.5%)		(80.5%)
	Total	20533				385352		7970242.2
		(100%)				(100%)		(100%)

state until the SCSI processor generates a TA in response to the $\overline{TS}$ generated by the arbiter. Once the TA is generated, the arbiter returns to state zero (see associated timing diagram in Figure 3c).

The latched signals $\overline{TS}$, TA, CS720, CSROM, and CSRAM must be cleared once the external arbiter reaches state 1.

Another dedicated bus application gaining popularity—RAID (redundant array of inexpensive disks)—can also take advantage of the improved throughput. A 53C720 would be assigned to each device in the array, and the devices that form the array would arbitrate over the dedicated bus for control of the bus. The design would simply require a more complex external arbiter, an address decoder, ROM, and RAM, in addition to the 53C720s. Although arbitration still occurs, it's limited to the dedicated bus, which frees up the system bus and results in lower overall system latency and increased performance for the RAID subsystem.☐

(Note: The figures and tables used in this article are for example purposes only. Consult NCR technical documentation for further design considerations and for the actual single- and multi-threaded SCRIPTS used in the calculations shown in Table 2a and 2b.)

Erik Paulsen, a SCSI application engineer with the NCR Microelectronic Product Division in Colorado Springs, Colorado, received his BSEE and MBA from the University of Colorado in Boulder.

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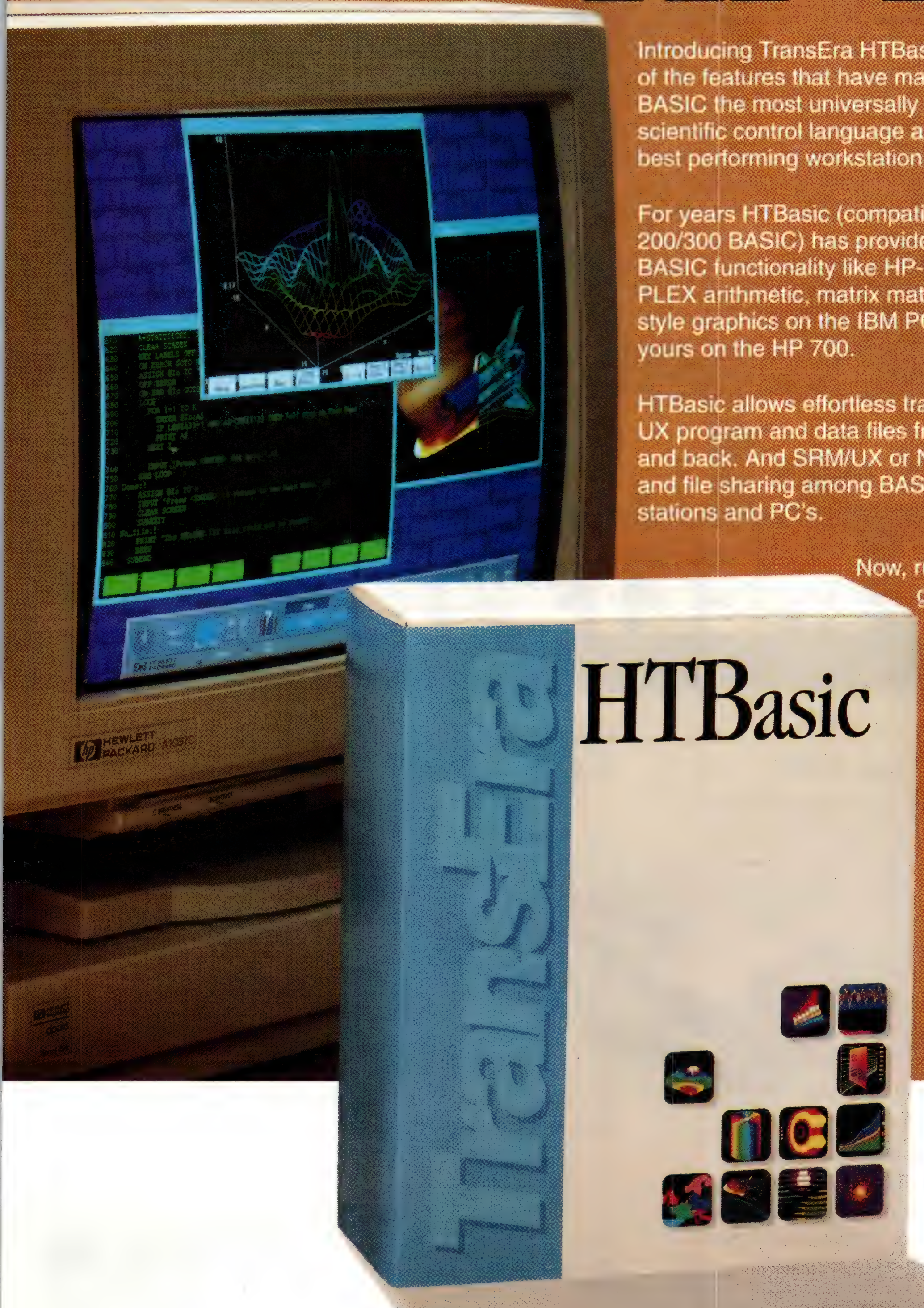

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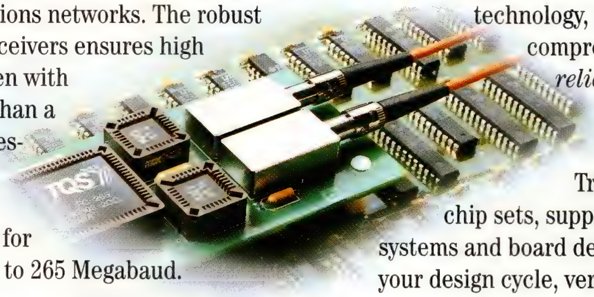


ELECTRONIC DESIGN

QUICK LOOK

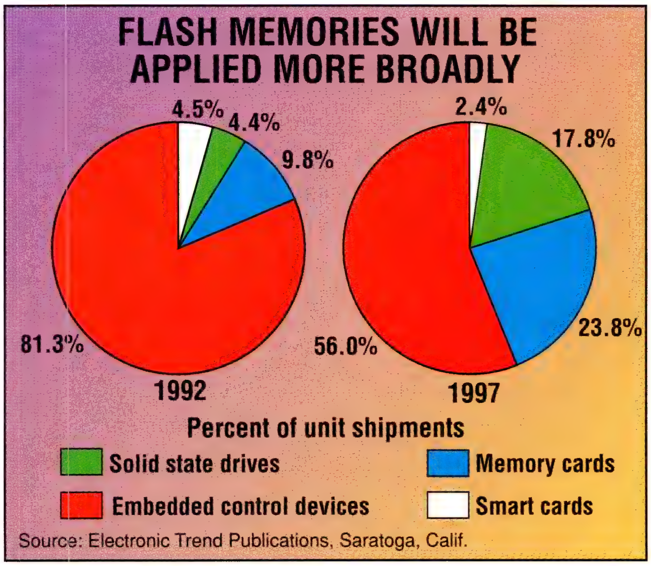
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

The world market for flash memory is expected to climb steeply in the next four years—this year's projected revenues of $250.2 million should grow to $2.967 billion in 1997. That's the estimate of Electronic Trend Publications. The Saratoga, Calif., market researcher explains that a new crop of higher density flash devices is responsible for fueling the expanding market. In particular, portable and mobile computers are well suited for memory cards and solid-state mass data storage devices.

Lower prices should enable flash memories to take on tasks done now by EPROMs and DRAMs. As a result, revenues for flash memory cards, which amounted to $49.0 million last year, should increase more than tenfold by 1997, amounting to $559.9 million by 1997.

Look for widespread acceptance of the 20-Mbyte flash memory cell array by 1994–1995, according to Electronic Trends, along with growth in ETOX (EPROM tunnel oxide process) flash technology, low-voltage, and select-erasure architectures.



Source: Electronic Trend Publications, Saratoga, Calif.

TIPS ON INVESTING

Four topics come to the forefront in an outline of the upcoming year for the municipal market: interest rate, taxes, supply, and demand. Long-term interest rates aren't expected to move much in either direction. Long-term municipal rates, however, could be the exception. Municipal rates may return to historical yields when compared to the other fixed income markets.

According to the Public Securities Association (PSA), long-term new-issue volume exceeded $274 billion in 1992. Why so much? As interest rates dropped throughout the year, issuers rushed to refinance much of their outstanding debt. As a result, more refunding issues came to the market in 1992 than in any other year. The PSA estimates about $185 billion in long-term bonds to be priced during 1993, a 20% drop compared to 1992.

It is difficult to say when a tax increase will take effect, but President Clinton's "Putting People First" campaign calls for an increase in federal taxes from the current 31% to 36% for individuals earning more than $150,000 and couples earning over $200,000 annually. While those affected are only a small percentage of the population, those same individuals, as investors, can move markets. Consider that if those investors buy more tax-exempt bonds in 1993 and fewer bonds exist, lower municipal interest rates may be inevitable.

Municipal bonds make economic sense for anyone currently in the 28% federal tax bracket or higher—in the 28% bracket, a AAA-rated 6% tax-free municipal bond is equivalent to buying a taxable bond yielding 8.33%. But more important, to fall into the 28% tax bracket an individual needs only to have taxable income of $22,101 or more. A couple filing jointly needs only $36,901 to fall into the 28% category. These numbers show that tax-free municipal bonds are not just for the rich any more. Another concern for taxpayers is that state and local taxes have increased 93% since 1982, according to *Money* magazine.

Use the following table to determine your federal tax bracket:

1993 federal income tax rates

Tax rate	Single taxpayers	Married filing joint returns
15%	0–$22,100	0–$36,900
28%	$22,101–$53,500	$36,901–$89,150
31%	$53,501 & up	$89,151 & up

Once you have determined your bracket, you simply need to know what your after-tax return is if you invest in a taxable investment. For example, assuming you buy a taxable bond yielding 8%, you need to know your return after paying federal taxes. Multiplying the 8% by the reciprocal on your bracket will give you the after-tax return: 8% X (100%–31%) = 5.52%

After paying federal taxes, the true after-tax return on the 8% taxable bond shrinks to 5.52%. Conversely, when considering a tax-free municipal bond, calculate the taxable equivalent yield (TEY). If the municipal taxable equivalent yield is higher than bonds currently available in the taxable market, the municipal bond makes sense. To determine the TEY, simply divide the municipal rate by the reciprocal of the tax bracket: 6%/100–31% = 8.69%.

Can you find as similarly rated taxable investment yielding more than 8.69%? If not, the municipal bond makes sense. Figures don't take into account the anticipated federal tax increase. For a 36% bracket, the new TEY would be: 6%/100–36% = 9.375%.

Henry Wiesel, financial consultant and investment counselor with Shearson Lehman Brothers, invites questions c/o Shearson Lehman Brothers, P. O. Box 8729, Red Bank, NJ 07001; (800) 631-2221.

WHAT'S NEW

NEW ACTIVE MATRIX LCD FROM SHARP ADVANCES FULL MOTION VIDEO.

Aiming at one of the 1990s' key market trends — multimedia computing — Sharp has developed a thin-film transistor (TFT) active matrix LCD that can reproduce not only computerized graphics, but also the animation and natural colors of video images, all simultaneously.

Compatible with VGA software, the new LQ10D311 produces 256,000 colors — a significant advancement over previous generation displays capable of just 512 colors. With 18 bits of information per pixel, the LQ10D311 achieves exceptionally high resolution and crisp, clear contrast. And its 80 ms response time is sufficient to display full-motion video right alongside the most demanding computer graphics applications.

Now available from Sharp offices nationwide, the LQ10D311 is targeted at high-end portable applications. As such, it meets requirements for reduced power consumption and lightweight, super-thin product design. Sharp's unique edge-lit style backlight, which reduces panel thickness to a mere 12.5 mm, also reduces power to remarkably low levels for truly portable operation.

IMAGINATION AT WORK

LOW POWER LOSS REGULATORS STREAMLINE DESIGN.

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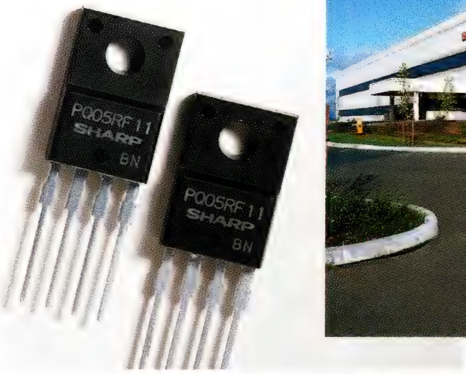
These are all benefits to be had from Sharp's innovative, 4-pin Low Power Loss Regulators. Their input/output voltage loss is a mere 0.5 V — versus the 2 V typical of conventional 3-pin voltage regulators — enabling reduction in the size, weight and cost of peripheral components.

Sharp's multi-function regulator line-up supports fixed and variable output, plus built-in ON/OFF control functions, reset signal generation and low current consumption at OFF state. Built-in overcurrent, overheating and short-circuit protection functions are included. And Sharp's compact package design — full mold or surface mount — means no isolation sheet is necessary.



SHARP IN THE U.S.A.

EXPANSION UNDERWAY AT U.S. HEADQUARTERS.

Reinforcing its commitment to U.S. customers, Sharp is adding 55,000 square feet of floor space earmarked for offices and light manufacturing at its Camas, Washington research and production facility.

Representing a $5.5 million investment, the addition will support continued expansion of flat panel technology and assembly for Sharp's growing U.S. market. The leader in LCD production worldwide, the company is poised to answer an expected increase in demand for Liquid Crystal Displays for the notebook and handheld computing marketplace.

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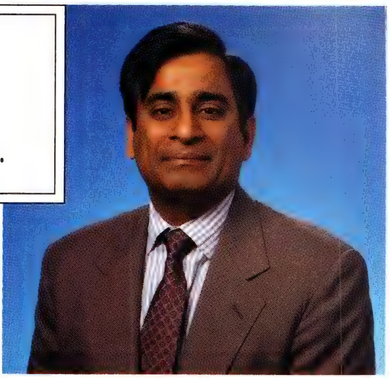
INSIGHTS FROM SHARP

FIRST PERSON

CCDs AND VIDEO IMAGING: LOOKING BIGGER ALL THE TIME.

VIJAY AULUCK
MARKET DEVELOPMENT MANAGER
MICROELECTRONICS GROUP
SHARP ELECTRONICS CORPORATION



Ask any number of people what "multimedia" is or should be, and you'll probably get as many different responses, encompassing everything from video teleconferencing to virtual reality. But one common denominator is the need for an image sensing and capturing device which emulates the human eye.

This is why Sharp has long pursued the potential of charge coupled devices (CCDs), the analog ICs first used in camcorders and now refined to provide higher performance in reduced sizes and weights. As such, CCDs have helped reshape the form and improve the function of established product lines — just witness today's 8 mm minicams, for example.

As a leading manufacturer of CCDs worldwide, Sharp supplies monochrome and color CCDs complete with peripheral drivers and signal-processing ICs, as well as camera modules. Newer chip sets offer dramatically enhanced sensitivities, compatibility with variable-speed electronic shutters, and arrays of almost half-a-million pixels.

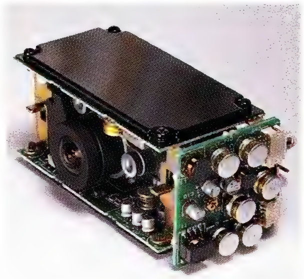
Video conferencing is just a first step for CCDs — in the PC area and beyond. You'll see CCDs expand into computer workstations as well as notebook and pen computers for applications to include real estate and insurance — video multiple listings, for example. And new applications limited only by your imagination are just around the corner: bar-code readers, video door phones, remote fingerprinting systems and rear view cameras where Sharp's unique implementation of the on-chip mirror image function enables ease of design and improved reliability.

With all this just a year or two away, and the multimedia market expected to skyrocket by mid-decade, it's no exaggeration to claim that today's smaller, lighter CCDs look very big indeed.

THE SHAPE OF THINGS TO COME

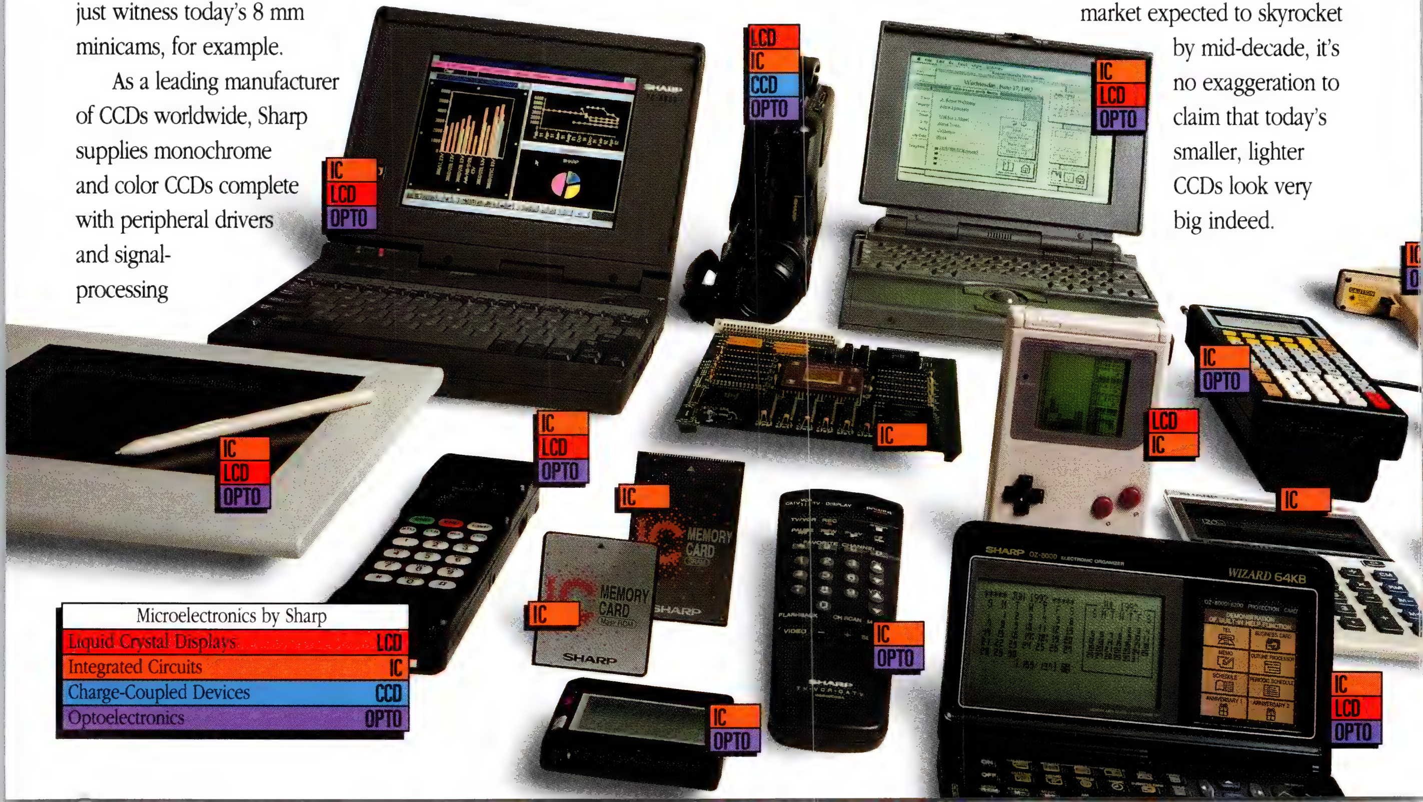
CCD MODULES: ALL ABOARD!

Currently under development at Sharp are color camera modules for customers whose applications involve a video camera, but who want to avoid design and development at the subassembly level. Instead, they can turn to Sharp for a low-cost, off-the-shelf solution — flexible and affordable enough to fit virtually any type of camera housing.



The modules consist of a CCD image sensor board with an integrated fixed focus lens, plus a video signal processing circuit board and 1 V peak-to-peak composite signal output connector terminal. Electronic iris control will allow the module to adjust automatically for the changing levels of illumination, even in low light conditions.

By providing all this in a compact, cost-effective package, Sharp's aim is to help streamline the design process dramatically — so that manufacturers of video cameras and other equipment can respond to new requirements and get to market with added value ASAP.



Microelectronics by Sharp	
Liquid Crystal Displays	LCD
Integrated Circuits	IC
Charge-Coupled Devices	CCD
Optoelectronics	OPTO

INSIGHTS FROM SHARP

MULTIMEDIA: THE BEST IS YET TO COME.

Even in an industry accustomed to one buzzword after another winning its 15 minutes in the spotlight, the appearance of "multimedia" products and technologies is generating real excitement. With the emergence of low-cost hardware capability and inexpensive mass storage, the market is catching up with a concept which has been a gleam in many an eye for years. Definitions vary — and could be argued for days — but Sharp takes a broad view of multimedia as digitized information drawn from two or more media, controlled on or by a computer with active user involvement.

Multimedia tools — including a CD-ROM drive, high quality display and appropriate operating system — can turn a personal desktop computer into a reference library complete with animation, photos and sound; a front row seat at an interactive analysis of Beethoven's *Ninth Symphony;* or a full-blown desktop business presentation center blending the best of computer, audio and video technologies.

To ensure depth and breadth of product line — and meet customer expectations successfully — Sharp's approach to multimedia is cross-divisional, encompassing display products, integrated circuits, optoelectronics and RF components. Advancements in each category are aimed at supporting new application development, overcoming cost constraints, and providing seamless integration.

THE "EYE" OF THE CAMERA.

CHARGE COUPLED DEVICES (CCDs) ARE A KEY PLAYER IN APPLICATIONS BASED ON CAMERA INPUT, USING AN ARRAY OF PHOTOSENSITIVE ELEMENTS TO CONVERT INCIDENT ILLUMINATION INTO A PROPORTIONAL ELECTRICAL CHARGE. ANTICIPATING DYNAMIC GROWTH IN MULTIMEDIA, SHARP NOW OFFERS 1/3″ CCDs WITH 410,000 AND 480,000 PIXELS, AND A 1/4″ DEVICE IS DUE LATER THIS YEAR. SENSITIVITY IS THE INDUSTRY'S BEST, REACHING 600 mV IN A NEW 1/3″ CCD WITH 270,000 PIXELS.

Though still in a state of relative infancy, the multimedia market is expected to reach mega-billion-dollar proportions in just a few short years. As stand-alone, network-assisted and broadcast-supported applications converge, and single chips approach not just one million, but 100 million transistors by the end of the decade, the PC is likely to be transformed into a pocket-size, CD-equipped companion/communicator. Great global digital highways will link its user to millions of people around the world. Heady stuff, but destined to build on today's seminal multimedia technologies and, if past is prologue, on components from Sharp.

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QUICKLOOK

OFFERS YOU CAN'T REFUSE

Intel Corp.'s PLDshell Plus V3.0 software is offered free of charge to designers who would like to evaluate the company's Flexlogic family of field programmable gate arrays (FPGAs). The Plus V3.0 software has language extensions to use the Flexlogic FPGAs, hierarchical design support, and fast-fitting algorithms for large FPGAs. It also has design entry, logic compilation, simulation, and programming software. For more information, write for Intel Literature Packet No. IP-108, P. O. Box 7641, Mt. Prospect, IL 60056-7641; (800) 548-4725 or (408) 765-6060. CIRCLE 451

A free disk demonstrates XL8, a tool to manage software translation. XL8, which eases the simultaneous release of software packages in multiple languages, maximizes the human translator's efficiency by automatically extracting and recompiling text strings while handling various character sets. XL8 runs under DOS but can work with software for multiple platforms such as Mac, Unix, Sun, Next, and so forth. Contact IDOC, 10474 Santa Monica Blvd., Suite 404, Los Angeles, CA 90025; (310) 446-4666. CIRCLE 452

A free compact disk (CD) from National Instruments demonstrates its LabView graphical programming software for the Sun Sparcstation. The LabView for Sun demo CD gives users a comprehensive look at LabView instrumentation. The demo package requires a Sparcstation 1 or higher with 24 Mbytes of main memory and 32 Mbytes of disk swap memory, Solaris 4.1.2, and Open Windows. Contact National Instruments, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100; fax (512) 794-8411. CIRCLE 453

A catalog from Computer Literacy Bookshops, the New Book Bulletin, gives brief reviews for new computer books on topics ranging from networking to system architectures and logic design theory all the way through fractal image compression and other graphics and animation subjects. The bulletin also has entry forms to win a trip to Silicon Valley (deadline is May 15, 1993) and details on contests to name the store's logo and a computer trivia contest (deadlines are May 15). Contact Computer Literacy Bookshops, 2590 North First St., San Jose, CA 95131; (408) 435-0744; fax (408) 435-1823; e-mail address is info @clbooks.com. CIRCLE 454

QUICK NEWS: SEMINARS

The Software Certification Institute is offering a three-day seminar on software safety. The seminar is the first of its type tailored to the IEEE software safety standard for companies wishing to comply with the IEEE standard or ISO-9000-part3. The institute will sell the class notes separately. Contact Leo Egan, P.O. Box 2328, Santa Maria, CA 93457; (805) 937-5383. CIRCLE 455

Of interest to design and manufacturing engineers, a course exploring engineering methods of cost evaluation of operations and products will be held June 8–10, 1993 in Memphis, Tenn. Contact Lourdes Carrion, American Society of Mechanical Engineers (ASME) Professional Development, 345 East 47th St., New York, NY 10017; (212) 705-7743, ext. J; fax (212) 705-7143. CIRCLE 456

KMET'S KORNER

...Perspectives on Time-to-Market

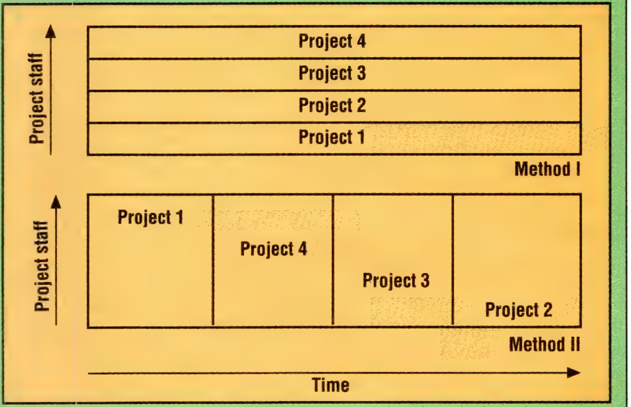
BY RON KMETOVICZ

President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

Concurrent engineering: Working on more projects than can be done all at the same time.

All too often development projects stretch out in time simply because they are not prioritized and thereby understaffed. To a first approximation, if a company is carrying two projects at one-half staff, each project will, on the average, take twice as long to complete. A creative firm that listens to its customers invariably is tempted to undertake more development work than it can digest. Thus, it is essential to know the firm's development capacity and to manage the start-up and prioritization of new projects with great discipline if development cycle time is to be minimized.

The company following the method I introduction plan currently works on four projects *(see the figure)*. Each of the four projects is staffed with one-quarter of the available staff so that four projects arrive on the market place at the same time. Or the company could dedicate staff to each project one at a time as shown by method II. This method outputs the first product in one-quarter the time; the second product in one-half the time, the third product in three-quarters the time; and the fourth product at the same time. Thus, three of four products show reduced cycle time as the remaining project exits at the same time.



The steady flow of product to market offered by method II has other benefits. One, it's much easier to introduce one product on a periodic basis than it is to launch four products at the same time. Two, the transfer to manufacturing is gradual—products flow into manufacturing rather than being dumped upon an already overloaded staff. Three, feedback from the market on Product 1 can be used to adjust Project 3; information from Product 4 helps shape Project 2; and feedback from Products 3 and 2 is used to adjust future projects. Four, engineering benefits by adding technology to products as it becomes available. Technological risk is greatly reduced! Fifth, a flow of new products motivates the team. People work smarter, faster, and better. Can you think of other good reasons for using method II?

QUICKLOOK

QUICK REVIEWS

Logic Design for Array-based Circuits reads like a cross between a textbook on structured design methodology and a practical guide for wending one's way through all aspects of circuit design for an array-based ASIC. Written by D. E. White and published by Academic Press, the book addresses the newcomer to application-specific IC design as well as the experienced circuit designer.

The first of 10 chapters has a review of different ASIC design approaches, various tradeoff issues, and a quick look at design tool choices. The ensuing chapters review structured design methodology, array evaluation and design sizing, design optimization approaches, timing analysis, power considerations (ac and dc), simulation approaches, and fault grading and detection.

Although the 343-page book uses a specific manufacturer's arrays—those offered by Applied Micro Circuits Corp., of San Diego, Calif.—the examples and approaches are generic enough to apply to a wide range of products. Many detailed examples throughout the book illustrate various tradeoffs, circuit approaches, and decision options that designers must go through to complete a design. Contact Academic Press Inc., 1250 Sixth Ave., San Diego, CA 92101-4311; (619) 231-0926, and ask for ISBN 0-12-746660-6.—*DAVE BURSKY*

CIRCLE 455

HOT PC PRODUCTS

MakeFast software automatically configures MS-DOS to make application software run as fast as possible. The program searches the hard disk to determine which software is used, then maximizes the memory available to these programs, supplying conventional, expanded, or extended memory for optimal performance. MakeFast has an introductory price of $29.95. Contact TDRMSoft, 275 West 96th St., Suite 10R, New York, NY 10025; (212) 865-2719. CIRCLE 456

To combat repetitive stress injuries in computer users, Forminco has come up with ergonomically correct products. The Mouse Arena pad elevates a mouse, keeping the wrist straight. With the company's adjustable computer furniture, users needn't leave the chair to remove pages from the printer or to send a fax. Prices are available on request from Forminco, 9610A Ignace, Brossard, Quebec, Canada, J4Y2R4; (514) 444-9488 or (800) 663-6764; fax (514) 444-9378. CIRCLE 457

ABOUT YOUR CAREER

The days of corporate loyalty and a-job-for-life may be over, but does that mean high turnover and low productivity must become status quo for American companies? For its part, Hewlett-Packard is increasing motivation and job satisfaction by helping its employees understand that they're responsible for advancing their careers and developing their skills—and giving them the tools to do so.

In 1986, HP's Roseville, Calif., unit began examining its career development process in response to employee concerns that managers weren't giving them adequate feedback. Jim Moore, manager of professional development programs, explains, "Career development efforts were OK, but we knew they could be better. We were looking for a tool to help us fine-tune the career development process."

HP's process helps individual employees and their managers clarify what the manager expects from the employee and the employee's personal strengths and development needs. It's used with managers and their direct reports at all levels and in all functions.

The career development process is widely recommended to employees at HP's Roseville site; however, with the exception of one business group, it isn't required. Of the 3,300 people eligible to participate, about 25 percent have done so, according to Moore.

Most important, says Pete Wyatt, support planning manager for HP's Support Materials Organization, the process has helped people define their interests and determine how they can be happiest and most productive in their careers.

"I use the methodology with every one of my people," he says. "In many cases, it has resulted in people becoming more effective and satisfied in the jobs they are in. In other cases, it's resulted in people changing jobs within the company."

One employee who participated in the process, called Managing Personal Growth (MPG), decided to take an in-house transfer with a temporary demotion. Recalls Wyatt, "We weren't happy with this employee's performance, and she wasn't happy with the job. After she participated in MPG, we ended up getting her a job as an administrative assistant in marketing. She's good with people. Today, she's a marketing engineer."

Wyatt says MPG, created by Blessing/White Inc., an individual and organizational development firm in Princeton, N. J., has even been the impetus for people who weren't satisfied with their jobs to leave HP. "One employee in a buyer-planner role had a part-time job at night tending bar and dreamt of owning his own club. Participating in MPG helped him clarify his values, and today he owns a club in Lake Tahoe," Wyatt says. The change was good for both the company and the employee.

While the MPG process is geared toward individual growth, it benefits the organization in a number of ways. For one, says Harry Gaines, chief executive officer of Blessing/White, "The participants begin to see their jobs as ways to fulfill their personal needs. They become more interested in improving their performance and their jobs."

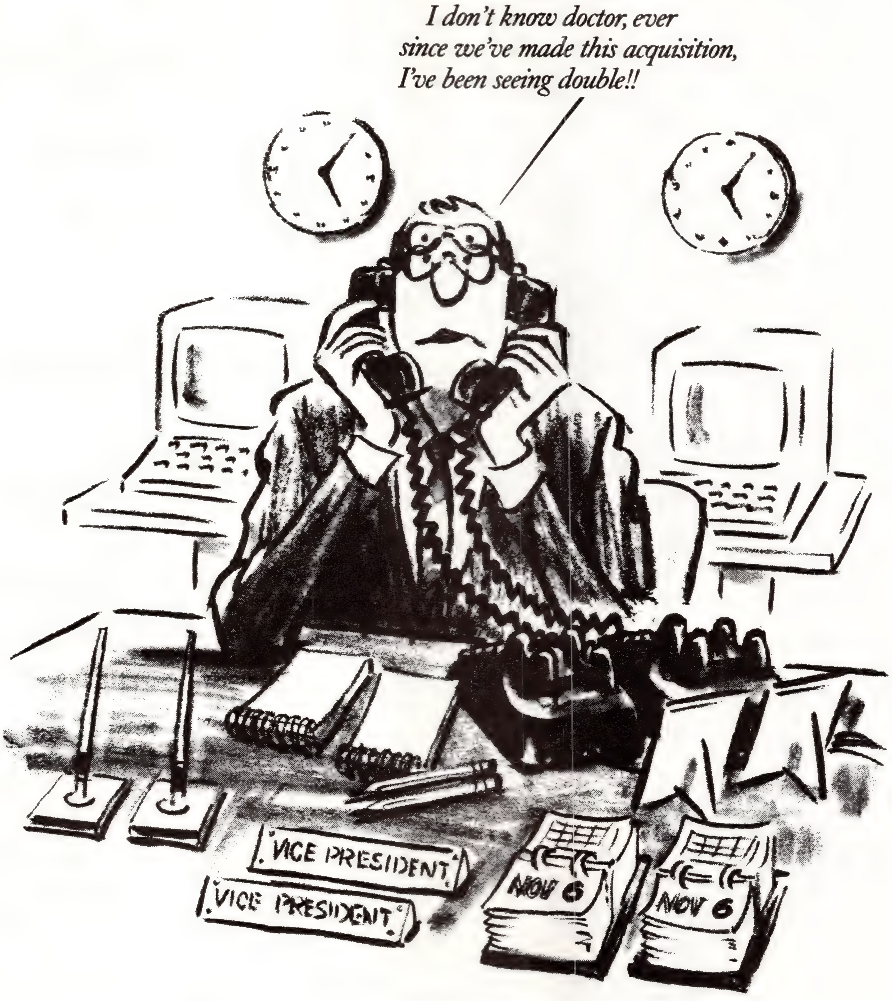
In addition, says Wyatt, the process benefits the company by encouraging employees to "own" their careers—and their jobs with HP. The process includes:

- Pre-workshop assignment. Each participant and his or her manager independently define the participant's job responsibilities, important skills and personal capabilities/talents.
- Employees also are asked to consider and rate their personal and professional values. They then are encouraged to think of their career growth in a new way, and to begin accepting responsibility for their success or failure.
- Participants attend a one-and-a-half to two-day workshop where they clarify their values and personal motivators and develop ideas for increasing job satisfaction. Here they also compare their priorities and skills with their manager's assessment of the same. With this in sight, they create a development plan outlining specific actions to increase job satisfaction and improve performance.
- The workshop prepares participants to initiate an honest, results-oriented discussion with their manager. The participant plans the agenda for and leads this discussion.

During the meeting, the participant and manager review the employee's development plan and agree on job priorities, area for development, and the best ways to use the employee's strengths. The open discussion, usually an hour to an hour-and-a-half in length, creates a partnership that helps promote individual and organizational success.

The development discussion differs from the performance appraisal conference by focusing on future development and encouraging two-way communication on topics initiated by employee. During the discussion, the boss plays the role of "coach" rather than "judge."

Manager and employee continue to meet two or three times yearly to talk about progress and plan for continuing development.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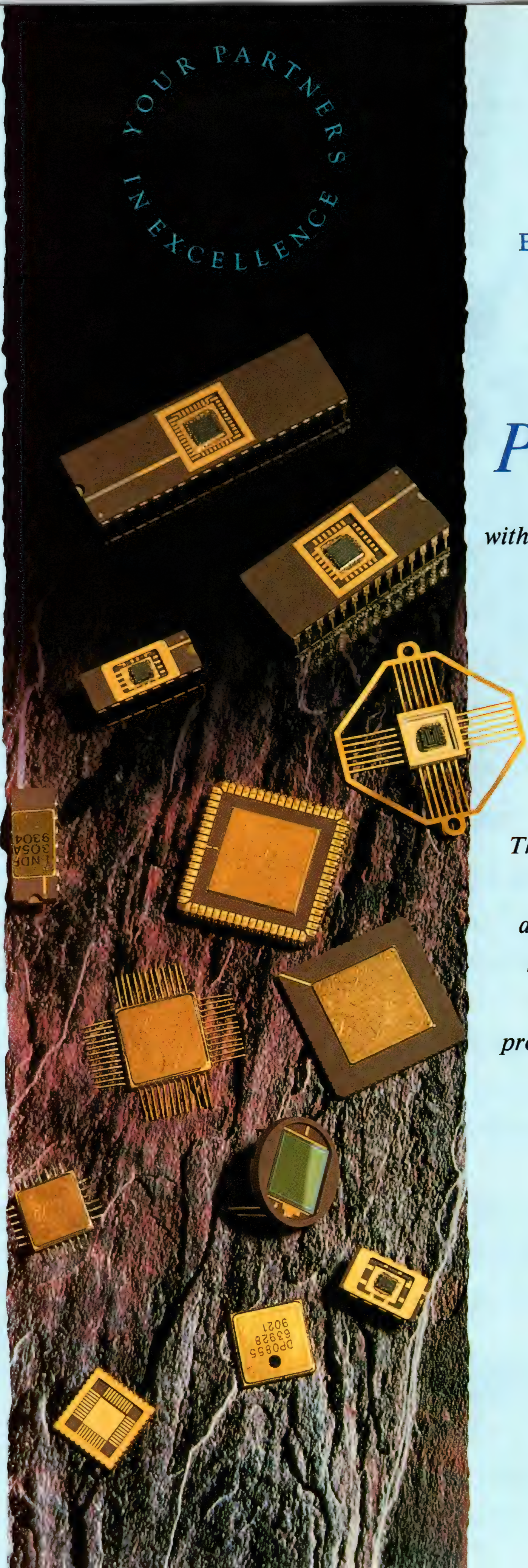

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CIRCLE

521 Fast Composite Amp Has Low Distortion

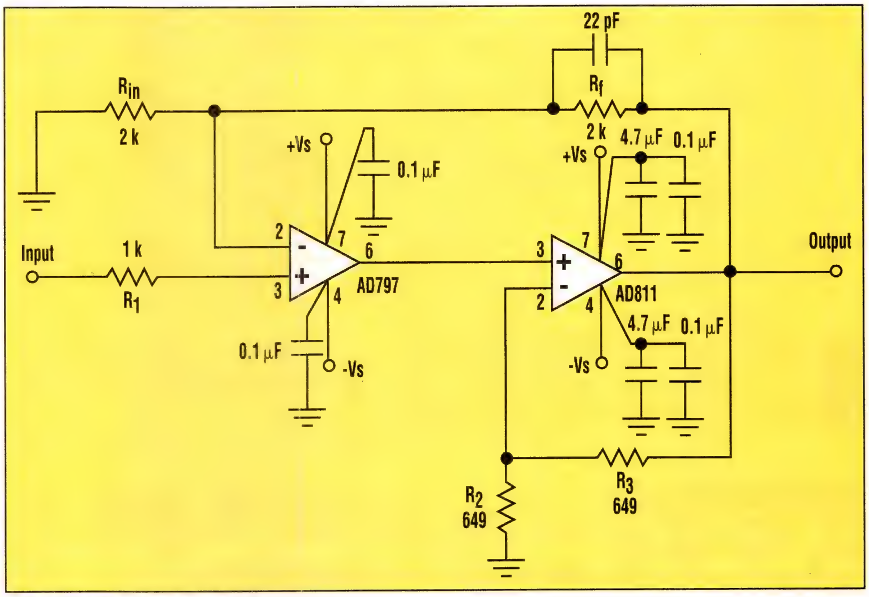
SCOTT WURCER and CHARLES KITCHIN
Analog Devices Inc., P.O. Box 9106, Norwood, MA 02602.

Although current feedback op amps offer high bandwidths over a wide range of closed-loop gains, they do have limitations. For instance, they typically have larger input offset errors and higher distortion at low gains than do comparable voltage feedback amplifiers.

By combining two op amps in a composite amplifier configuration, this circuit *(see the figure)* can overcome those disadvantages and achieve high performance. Here, an ultra-low-noise, low-distortion op amp—the AD797—is combined with the AD811 op amp, which offers a high bandwidth and a 100-mA output drive capability. The composite-amplifier circuit serves quite well when driving high-resolution ADCs and ATE systems.

The fast AD811 operates at twice the gain of the AD797 so that the slower amplifier need only slew one-half of the total output swing. Using the component values shown, the circuit is capable of better than –90 dB THD with a ±5-V, 500-kHz output signal. If a 100-kHz sine-wave input is employed, the circuit will drive a 600-Ω load to a level of 7 V rms with less than –109 dB THD, as well as a 10-kΩ load at less than –117 dB THD.

The device can be modified to supply an overall gain of 5 by changing both the R_F/R_{in} ratio and R_3/R_2 ratio to 4:1. This raises the gains of AD811 and the total circuit while maintaining the AD797 at unity gain. If only the R_F/R_{in} ratio is changed, the circuit may become unstable. In contrast, if only the R_3/R_2 ratio is varied, the AD797 will then operate at gain. Subsequently, the circuit will have a lower overall bandwidth. R_1 should be equal to the parallel combination of R_{in} and R_F.☐



A COMPOSITE amplifier with an ultra-low distortion can be created by combining two op amps, which in this case are the AD797 and AD811. With the given component values, the circuit is capable of a -90 dB THD with a ±5-V, 500-kHz output signal.

IFD WINNER

IFD Winner for January 7, 1993

Mike McNatt, Amoco Technology Co., P.O. Box 3011, Naperville, IL 60566-7011; (708) 961-6296. His idea: *"One Pot Adjusts Polarity, Gain."*

CIRCLE

522 Chop DC Output To Get AC Standard

M.J. SALVATI
Flushing Communications, 150-46 35th Ave., Flushing, NY 11354.

Voltage standards for ac are rarely found outside a metrology lab. However, a crude yet effective way to rig a source of known ac voltage is to chop the output of a known dc voltage source. Either a dc voltage standard or a stable dc supply monitored by a 4-digit DVM can be used as the source of known dc voltage.

Any dc voltage source in the 2-to-15-V range can be chopped into a unipolar square wave that has a peak amplitude nearly equal to the dc source voltage with this circuit (lightly loaded CMOS will swing within a few millivolts of each rail at low frequencies) *(see the figure on p. 94)*.

Depending on the actual voltage of the supply, the programmable-unijunction-transistor (PUT) relaxation oscillator produces 1600-2000 Hz trigger pulses. These pulses operate the cascaded 74C107 flip-flops, producing a square wave whose fre-

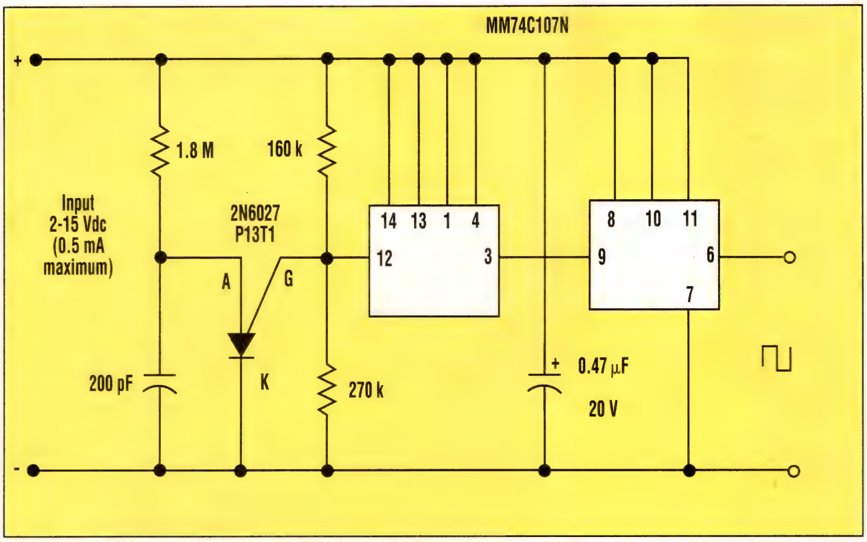
INTERNAL METER COUPLING

Meter rectifier type	DC	AC
Average responding	2.000	2.000
Average responding, rms calibrated	1.800	1.800
True rms	1.414	2.000
Peak	1.000	2.000

quency is around 400-500 Hz.

The chopper's unipolar square-wave output can be used to check the calibration accuracy of any scope or ac voltmeter, as long as the type of meter response and its internal coupling is known. The proper correction factors for the major meter-rectifier types and each kind of coupling is given *(see the table on p. 93).*

Although you can set the dc source for the desired calibration voltage and multiply the meter reading by the correction factor, it's easier to set the dc source to the product of the desired ac voltage and a correction factor. For example, if you have an average-responding, rms-calibrated voltmeter (most common over the past 80 years) and want to check the calibration at 5 Vac, set the dc voltage source at 5.00 × 1.8 = 9.00 Vdc.☐



USING THIS CHOPPER CIRCUIT, any dc voltage source in the 2-to-15-V range can be chopped into a unipolar square wave with a peak amplitude that's nearly equal to the dc source voltage, thus creating a known ac voltage.

CIRCLE 523

CALCULATE AC WATTS WITH VOLTMETER

IRWIN COHEN
Hewlett-Packard Co., Clinical Systems Business Unit, 175 Wyman St., P.O. Box 9030, Waltham, MA 02254-9030.

Measuring ac power doesn't necessarily require special equipment. In many cases, all that's needed is a high-input impedance ac voltmeter, followed by a few simple calculations.

The problem basically consists of determining the power factor of the load—the cosine of the phase angle between the voltage across the load and the load current. Using a simple circuit *(Fig. 1)*, that angle can be calculated quite simply.

The circuit uses a 1:1 isolation transformer to prevent direct contact with the line. It is wise to proceed with caution whenever voltages of this magnitude are utilized in a test setup, even though the voltages that will be measured are usually below 1 V.

R_s is a current-sense resistor and R_r is a multi-turn potentiometer. The voltage across R_r is approximately 0.5% of the line voltage, which should be sufficient for most applications.

R_r is adjusted so that $|V_r| = |V_s|$; then V_d is measured. In the vector diagram *(Fig. 2)*, according to Kirchhoff's voltage law, V_s, V_d, and V_r form a triangle, which becomes isosceles by adjusting R_r. V_s is in phase with the load current and V_r is essentially in phase with the load voltage.

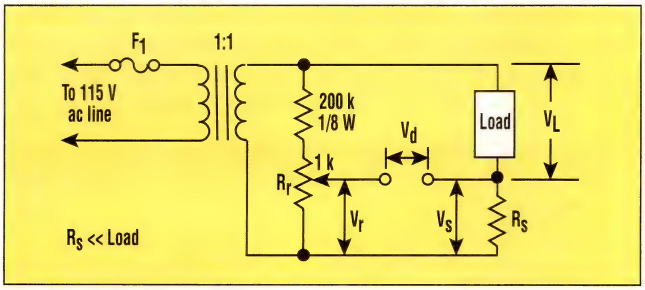
The power delivered to the load can be calculated as follows:

$$P_L = V_L \times I_L \times \cos\theta$$

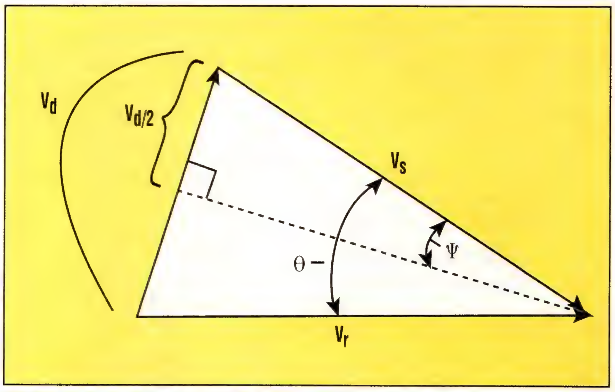
$$= V_L \times (V_s/R_s) \times$$

$$\cos[2 \sin^{-1}(V_d/2V_s)]$$

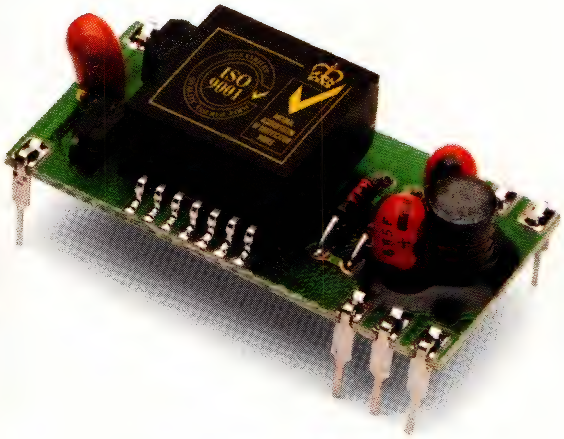
$$[\theta = 2\psi = 2 \sin^{-1}(V_d/2V_s)]$$ ☐



1. THE LOAD'S power factor, which is the cosine of the phase angle between the voltage across the load and the load current, can be calculated simply with this circuit. A 1:1 isolation transformer is used to prevent direct contact with the line.



2. BY PROPERLY ADJUSTING R_r, the vector diagram of voltages V_s, V_d, and V_r forms an isosceles triangle, which simplifies the power calculation.



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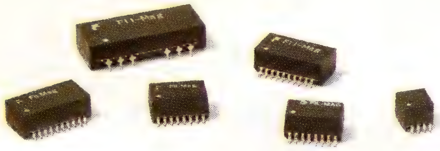

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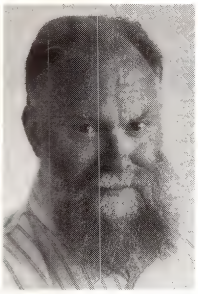

BOB'S MAILBOX

Dear Bob:

This letter is in response to your August 20, 1992 article titled *"What's All This Spreadsheet Stuff, Anyhow?"*

There is nothing wrong with the Spreadsheet! The problem is with the user of the spreadsheet. Back when we trained our engineers to use slide rules for their calculations, the first thing we learned was about accuracy. We all learned how to do complex calculations but understood the limits of the slide rule's accuracy.

Unfortunately, in business school there is no caution about the accuracy of the trusted spreadsheet. The problem with the spreadsheet is less with the tool than the person using the tool. The spreadsheet is an outstanding tool when put to use by a person who understands the limits and proper application of the tool.

V.A. CLAUDE
Orlando, FL

Yeah, nobody does a sanity check on their computers—sigh!—RAP

Dear Bob:

I do not quite agree with your views about spreadsheets. I have been using spreadsheets (computer spreadsheets) for the last 5 years and I have found numerous uses, which could not be done by hand calculation. The following are some examples.

To look at parametric distributions of a particular product, frequency distributions and trend charts can be produced very easily by using spreadsheets. These by the way, give a precise picture of what the product does, and this can not be seen by just looking at numbers. To fine-tune a process to get optimum performance and yield, such data is not only useful but necessary.

The distribution plots and trend charts make a lot of business decisions very easy, and no one's personal judgment and experience is necessary. The data speaks for itself. The distributions can also be used for competitive product analysis, which tell you exactly where you stand with your competitors. This type of data analysis gives you a direction for improving the product to make it more competitive or even to set goals for new products.

The statistical data analysis becomes very easy with the use of spreadsheets. Pareto analysis of failures points to the most critical problem and also indicates all other problems in order of importance. The simple data sorting of failure categories would be an enormous task if one wants to do it manually. Also, the facility of importing data from automatic test equipment simplifies the analysis process. The Paretos are not only useful in technical analysis, but in business planning as well. The volumes of numerous products can be compared at the same time and forecasts made based on the facts. The products that are not selling well are also identified at the same time, and the sales force can be given the directive to focus on those. The same technique can be used to monitor expenses and control spending on all of the things involved in managing a business.

Thus, there are plenty of very good uses for spreadsheets, in technical as well as business areas. And spreadsheets do not endanger corporate health at all. The complaint in your article could be applied to any machine. We must remember that machines can not think. If a human being makes a mistake, they will repeat it or may magnify it. But, there has to be a human error involved. If there is no human error, there is nothing to complain about—but there is a lot to benefit from today's machines (including computer spreadsheets).

ABHIJIT TULPULE

Oh, yes, you are surely right, spreadsheets do things that otherwise would be ABSOLUTELY IMPOSSIBLE; no judgment necessary.—RAP

Dear Bob:

I always enjoy your column and have been tempted to stick my oar in before now. But I don't see how I can let this Spreadsheet subject go by without some comment.

First, your examples concerning ROI and frequency optimization bring just one word to mind: GIGO. Sure, you can get incorrect answers with a spreadsheet—but I can get answers, probably even MORE incorrect, with pencil and paper. Let's not blame the poor spreadsheet because someone feeds it garbage.

Second, what kind of accuracy do you get from a slide rule? Better than a spreadsheet? What KIND of spreadsheet?

Finally, you are right about the spreadsheet only thinking (my apologies) linearly. Computers in just about any application aren't worth a toot at being creative, which sounds like what you and Schrage were talking about. But be reasonable—my hammer doesn't do a real good job of removing chips from a circuit boards, either, but I still find uses for it~! Maybe it's a question of the right tool for the right job...

Keep the columns coming!

BILL AULL
Technical Director
WLTX TV
Columbia, S.C.

That reminds me of the old saying, "To a man with a hammer, everything looks like a nail." To a man with a computer, everything looks like—a computer problem!—RAP

Dear Bob:

I read your article concerning spreadsheet mentality with great interest. What you have observed is considerably more significant than you may realize.

The spreadsheet permeated the real estate valuation industry originally as the Ellwood Method about 30 years ago and more recently (15 years) as Discounted Cash Flow Analysis.

A fundamental mathematical formula expresses the relationship of the three variables involved when valuing an income stream:

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Y = R + A, where:

Y = Discount or Yield Rate (annualized rate used to equate future income to present value); R = Capitalization Rate (rate of annual income); A = Growth Rate (rate of annual growth).

The appropriate Discount Rate for valuing an income stream equals the Capitalization Rate plus the Growth Rate.

Spreadsheet valuation programs let the user treat these three interdependent variables as if randomly independent. Once two variables are input, the third is, of course, determined.

If the Discount Rate is mathematically understated, or the Growth Rate is mathematically overstated, the value produced by the spreadsheet is mathematically inflated. In either case, the *present value* of increasing income is overstated.

Milton Friedman argues academically that the possibility of an exception (i.e. a property *could* outperform the market) means that the formula for valuation of an income stream is not necessarily hard and fast.

How would you like to be a stockholder in a Savings & Loan where *every* loan was predicated on the collateralized asset outperforming the market? This is what happened and half the Savings & Loans are no more.

There have been those in my industry who have specialized in such distortions, which is THE reason for the Savings & Loan crash.

Your observation was particularly interesting to one who has been making a similar argument in a seemingly unrelated field for the past twenty years.

MICHAEL D. HARTNETT
Tampa, Fla.

Yeah, everybody making the SAME assumptions and using the SAME spreadsheet—right or wrong—is scary all by itself! "Every loan must outperform the market"... Wow!—RAP

Dear Bob:

You've done it again—written about something I just *have* to comment on even though I'm supposed to be doing real work.

I, of course, refer to your heroic efforts to maintain charge on your camcorder battery while in the field. Your existing solution is ingenious and reliable, but an hour's worth of whirring noise while sitting around a wilderness campfire must take a little bit of the charm out of the experience.

My thoughts are as follows:

1. I think you dismissed the option of using a set of D cells too quickly. Good Alkaline D cells have 14 Ah of capacity—about 3 to 4 times that of lead or Nicad. Although we need to confirm (by testing) whether you can draw 1 A from a D cell for the whole 14 hours, it seems reasonable to expect a week of shooting at one hour a day. A second set of cells will carry you for another week, at a total weight comparable to your generator set. A drawback, of course, is the extra wiring from your belt pack to the camcorder.

2. High rollers (like networks) are said to use primary lithium batteries, which should double or triple the life of alkalines. This option will probably not appeal to your penurious nature.

3. If you really prefer recharging the built-in battery, what about those thermoelectric generators the Soviet Army was supposed to have used? Campfires (or lanterns) are always available on camping trips, and this would be a silent and effortless option. I'm sorry I don't know more specifics, but the modules used for automotive coolers might well supply useful power at a reasonable voltage.

4. If you aren't already aware, the biggest problem in field use of camcorders is the prevention of internal dust and especially internal condensation. A "dew" episode will, at the minimum, trigger a protective shutdown that lasts an hour or more and may well drain your battery (the camera is supposed to stop and warm itself to drive off the moisture). Any attempt to bypass this protection will result in severe head clogging and tape damage (I spent several hours with the hair dryer on a cruise ship hand drying the tape inch by inch after taking my camcorder out of an air-conditioned cabin into Gulf Stream humidity, and misinterpreting the "Dew" warning as a low battery indication that I apparently overrode by changing batteries). While your treks don't seem to feature air conditioning, cameras carried next to perspiring bodies can suffer similar problems. Make sure your fanny pack is sweat-proof.

5. One more tip—are you *sure* you want an hour a day of footage? Even if it's all gorgeous, consider how long it will take you to watch the final product; maybe you should be a little more judicious on the trail. I took almost 6 hours of footage on a truly unforgettable Orient Express train tour from Paris to Istanbul in 1984. It's all good stuff but hard to show to anybody due to its length. You would have been impressed by my efforts. This was the pre-camcorder era—I lugged a portable deck whose "compact" camera alone was bigger than most of today's camcorders. The train was advertised as using authentic '20's era cars, so I suspected that ac power might not be available. They did say that each compartment had a small fan. I built a "universal" charger using a capacitor to limit the current at 220 V ac to 100 mA, so I could get something off any ac voltage (primarily for hotel room use). However, I correctly surmised that the train's lighting power would be dc, because old train cars used storage batteries recharged by belt-driven generators running off the wheels. Having thoughtfully provided myself with a meter, tools, and a dropping resistor, I determined that the fan was powered by 28 V dc and could readily be tapped at a screw terminal block, like the ones in your old VW. I was not only able to recharge my spare battery, but was able to power my "12-24 V" 7-in. TV, so we could see the "dailies" in the comfort of our compartment. A 16mm film crew had taken the trip earlier, and a network crew had made at least a partial trip, but I expect I was the first consumer video shooter to go the distance.

Good luck with your efforts—modern camcorders are wonderful memory-savers, although not as robust as film cameras.

Patrick H. Quilter
Vice President of Engineering
QSC Audio Products
Costa Mesa, Calif.

Thanks for the tip on alkaline cells. I'm investigating thermoelectric generators (heavy and inefficient?). I love your story of 28 V dc on the train!—RAP

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PLUGGING INTO PCMCIA

PC CARD ATA SPECIFICATION

STEPHEN GROSS, SUNDISK CORP. AND LEVI LEBO, HEWLETT-PACKARD CO.

The PCMCIA PC Card ATA (AT Attachment) specification makes removable rotating-disk and solid-state storage devices a viable medium for storing data in portable systems. This specification works with the existing ANSI ATA standard. These types of removable drives are available with various cost, performance, ruggedness, and power-consumption levels. But most importantly, any of the drives that adhere to the specification are interchangeable when used in a PC Card ATA-compatible slot.

Notebook computers are commonplace today, while subnotebooks and palmtop computers are gaining popularity. In addition, credit-card-sized removable-storage and communications cards based on the PCMCIA 68-pin card standards are beginning to proliferate. The first subnotebooks and palmtop computers used either Type 1 (3.3-mm thick) or Type 2 (5-mm) cards for their primary mass storage. Though the original PCMCIA interface was envisioned solely for solid-state storage media, the use of rotating-disk cards is made possible because of the recent release of version 2.01 of the PCMCIA standard. This release incorporates a Type 3 card (10.5-mm) as well as the PC Card ATA specification (1.01), which is also referred to as PCMCIA-ATA.

The PC Card ATA specification maps the ATA (sometimes called IDE, or integrated-device electronics) hard-disk-access protocol onto the PCMCIA interface for the removable storage devices. This single, stable protocol is needed to supply interchangeability between solid-state and rotating-media storage cards, as well as between similar products from different vendors or from one generation of card to the next. This contrasts with conventional flash-memory PCMCIA cards whose programming algorithm varies between vendors.

Even though new, proprietary file systems are usually required to take advantage of conventional flash-memory cards, the PC Card ATA standard supports the traditional 512-byte blocks used by today's file systems. Systems that support PC Card ATA-compatible peripherals make the storage device's configuration transparent to the end user. Field upgrade or reconfiguration is done automatically because each drive reports its characteristics to the system through its PCMCIA Card Information Structure (CIS) and the ATA Identify Drive command.

The PCMCIA specification defines an interface between the host-system bus and the peripheral controller card. The ATA standard defines a set of controller registers and the protocols that explain how to access them. The ATA registers reside in the drive but effectively sit on the system bus and are thus suitable for PCMCIA. Other drive interfaces that define a controller-to-drive connection, such as SCSI, ESDI, or ST506, require standardization around a specific controller implementation.

The ATA protocol defines ten active I/O ports in two groups. These groups are usually placed at I/O addresses 1F0 to 1F7 and 3F6 to 3F7 in a PC/AT system's I/O space. The PC Card ATA standard supplies four basic addressing modes for access to the registers: Memory and Primary, Secondary, and Contiguous I/O.

The Primary and Secondary modes supply the exact mapping to I/O addresses used for IDE drives in existing BIOS implementations. For new designs, the Contiguous-I/O and Memory-mapped modes let the host system select the ATA register's base address with its socket controller to minimize address conflicts. With all four modes, the interrupt signal can be routed to any interrupt level supported by the host socket. The optional Memory-mapped mode of the PC Card ATA specification allows cards to be used in PCMCIA Release 1.0-compliant sockets that don't offer any I/O support.

Optional Master-Slave operation at the Primary and Secondary addresses is defined, although the protocols are slightly different than those in the ATA specification. This is because the –PDIAG (Passed Diagnostics) and –DASP (Drive active/Slave present) signals aren't available on the PCMCIA interface.

Master-slave operation and addressing-mode selection is accomplished without any jumpers or switches on the card. The host software selects the best configuration for its environment from the choices provided by the card's CIS.

Card insertion and removal is detected by a pair of Card-Detect pins on the PCMCIA interface. The recently released PCMCIA Card- and Socket-Services specifications define two software layers that support host-socket configuration and selection of the card's operational mode. These layers notify a driver when a card is inserted or removed.

For more information on the PC Card ATA spec or other PCMCIA-related issues, contact the PCMCIA (408) 720-0107. The ATA draft ANSI standard containing details on the registers and protocols for PC Card ATA-compatible hardware and software can be purchased from Global Engineering. Contact them at 800-854-7179.

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SYSTEM DESIGN NEWS

A cross-operating-system tool interface (TIS) released at Software Development '93 promises to advance the interoperability and portability of application development tools. The standard's committee will study the interfaces that are visible to software development tools used by 32-bit PC applications developers. Furthermore, the members will agree on a standard set of tool interfaces to enhance the interoperability and portability among the tools provided by TIS-compliant vendors. The standard should improve the delivery of application software for 32-bit Windows, OS/2, and Unix operating software, as well as other operating-system environments.

Portable standards selected by the TIS committee include the first linkable, loadable, and debug format interface specifications, which they hope the industry will standardize on. Portable formats selected as a TIS include the OMF (relocatable object module format), ELF (executable and linkable format), and DWARF (debug with arbitrary record format). Formats selected for Microsoft's Windows' environment include Microsoft's PE and Symbol and Type Information (MS STI). The founding members of the TIS committee include Borland, IBM, Intel, Lotus, MetaWare, Microsoft, The Santa Cruz Operation, and Watcom. Copies of the TIS specification are available from Intel Corp., Santa Clara, Calif. Call them at (800) 548-4725 (request item number 241597), or use the Intel Access on CompuServe.

Developing applications for Microsoft's Windows operating system is made easier with a collection of 19 custom controls with which developers can create eye-catching 3D controls (such as text boxes, buttons, and window frames). Used with Microsoft's Visual C++ development system or the company's Visual Basic programming environment, the tools allow developers to quickly add to various applications functions, including charting, communications, and multimedia capabilities. The Visual Control Pack from Microsoft Corp., Redmond, Wash., eliminates the need for developers to continually "re-invent the wheel" with modular, prebuilt controls. As a result, developers can concentrate on the core applications.

The software package includes a half-dozen 3D controls; a graphing tool; a serial-port communications tool; common dialogue; gauge control; multimedia; several pen controls; animation, spin, and PicClip for image manipulation; and Keystatus to set and display the state of various keys. The Visual Control Pack has a list price of $149. Contact Microsoft at (206) 882-8080.

A software licensing scheme that provides invisible security and a wide range of flexibility lets software suppliers track and control software, even if sold by third-party distributors. The security package from Kentronic Controls Ltd., Calgary, Alberta, Canada, protects a software package from unauthorized use and copying. It can grant customers: up to 65,000 levels of privileges, usage privileges limited by time or number of uses, and all turnkey software-usage privileges. And it all can be done over the telephone.

The CrypKey software doesn't need a hardware key or disk key, but uses a combination of computer hardware and sophisticated encryption algorithms. The package includes a software library that easily integrates with the developer's existing programs. Included in the product library are 10 simple-to-use function calls that can be added to application packages, turning them into fully license-controllable packages. Once attached to an application program, the CrypKey software can't be copied by any disk-copy programs. The security program prevents the application from running until it's authorized to do so. Warning actions can range from a simple annoyance dialogue box to request authorization, to full program shutdown. Contact Jim McCartney, (403) 258-6225.

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The 8540-RV is a rack-mount industrial computer with a built-in, 14-in. Super VGA (SVGA) monitor. The backplane contains ten full-length board slots. The chassis can also hold baby AT motherboards. The front panel contains the keyboard connector, reset button, and on/off switch, all of which can be locked behind a secured door. The card-cage area is mounted to the rear of the CRT cage and is hinged for easy access from either the front or the rear of the unit.

The housing has enough room for two 5-1/4-in. drives and one 3-1/2-in. drive. The 8540-RV-10 lists for $3995 and includes the chassis, backplane rack slides, and monitor. The 8540-RV-8MB costs $3895 and comes with the chassis, mounting hardware for a motherboard, rack slides, and monitor.

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▼ CD-ROM DRIVES TRANSFER 150 OR 300 KBYTES/S

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The model 38, which has a small footprint and weighs just 2.2 lbs, boasts an average access time of 400 ms. Its flow-through 64-kbyte cache memory supplies smooth motion video. The models 74 and 84 each come with 256 kbytes of cache memory to sport a 280-ms access time. Prices for the 38, 74, and 84 are $465, $615, and $550, respectively.

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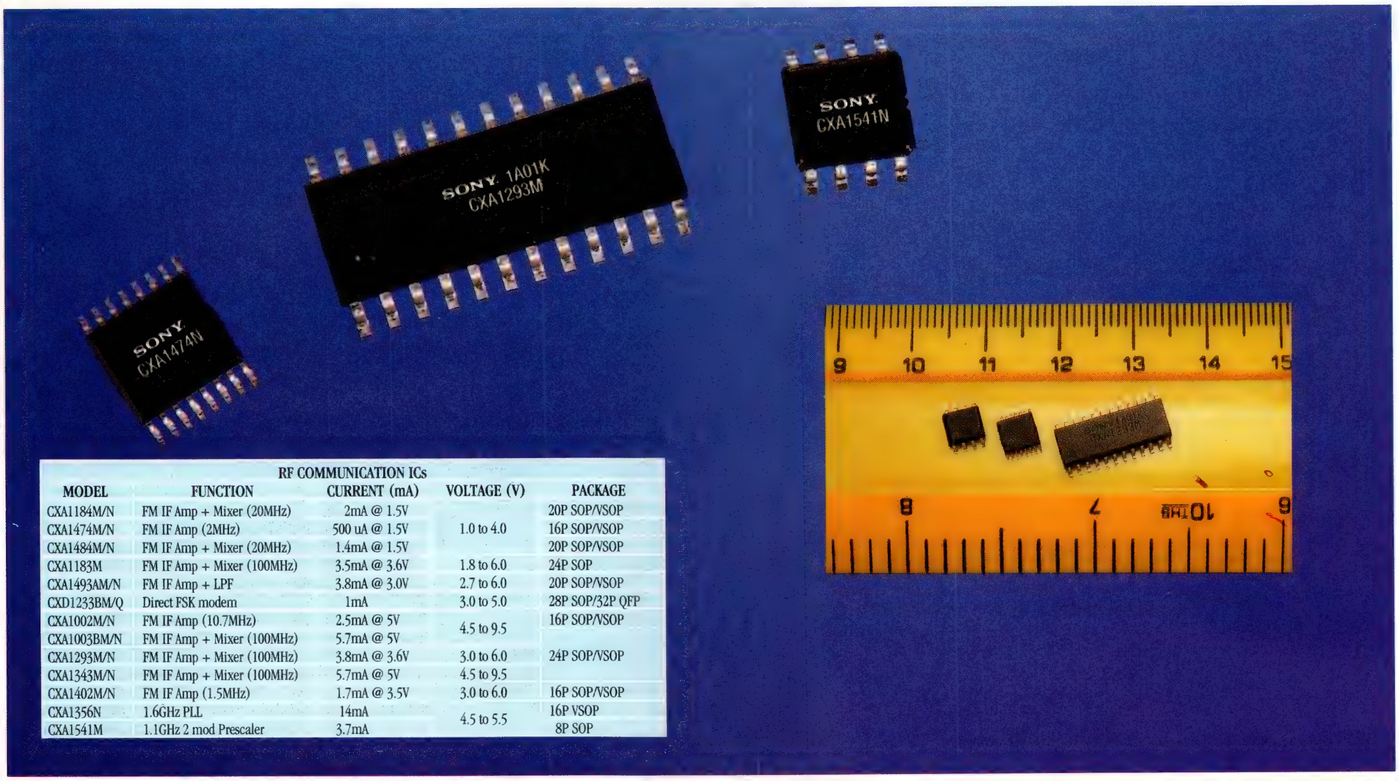

RF COMMUNICATION ICs

MODEL	FUNCTION	CURRENT (mA)	VOLTAGE (V)	PACKAGE
CXA1184M/N	FM IF Amp + Mixer (20MHz)	2mA @ 1.5V	1.0 to 4.0	20P SOP/VSOP
CXA1474M/N	FM IF Amp (2MHz)	500 uA @ 1.5V		16P SOP/VSOP
CXA1484M/N	FM IF Amp + Mixer (20MHz)	1.4mA @ 1.5V		20P SOP/VSOP
CXA1183M	FM IF Amp + Mixer (100MHz)	3.5mA @ 3.6V	1.8 to 6.0	24P SOP
CXA1493AM/N	FM IF Amp + LPF	3.8mA @ 3.0V	2.7 to 6.0	20P SOP/VSOP
CXD1233BM/Q	Direct FSK modem	1mA	3.0 to 5.0	28P SOP/32P QFP
CXA1002M/N	FM IF Amp (10.7MHz)	2.5mA @ 5V	4.5 to 9.5	16P SOP/VSOP
CXA1003BM/N	FM IF Amp + Mixer (100MHz)	5.7mA @ 5V		
CXA1293M/N	FM IF Amp + Mixer (100MHz)	3.8mA @ 3.6V	3.0 to 6.0	24P SOP/VSOP
CXA1343M/N	FM IF Amp + Mixer (100MHz)	5.7mA @ 5V	4.5 to 9.5	
CXA1402M/N	FM IF Amp (1.5MHz)	1.7mA @ 3.5V	3.0 to 6.0	16P SOP/VSOP
CXA1356N	1.6GHz PLL	14mA	4.5 to 5.5	16P VSOP
CXA1541M	1.1GHz 2 mod Prescaler	3.7mA		8P SOP

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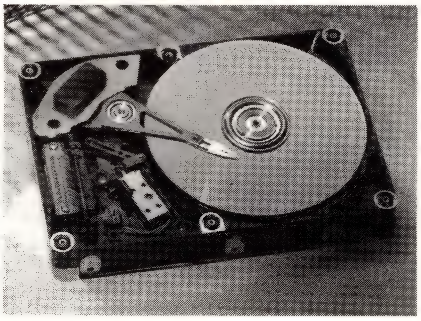
CIRCLE 198 FOR U.S. RESPONSE CIRCLE 199 FOR RESPONSE OUTSIDE THE U.S.

▼ DRIVES' SCSI INTERFACE PUSH 20 MBYTES/S



A series of 1-in.-high drives combine a common SCSI code set with both fast and wide interfaces. With their 8- and 16-bit single-ended and differential SCSI-2 electronics, data-transfer rates of up to 20 Mbytes/s can be achieved. Three models are currently available: The DSP3133L has a capacity of 1.33 Gbytes, the DSP3107L holds 1.07 Gbytes, and the DSP3053L stores up to 535 Mbytes. The 5400-rpm and 512-kbyte segmented cache buffer result in an average seek time below 9.5 ms and an average latency of 5.6 ms. Typical operating power for the drive is about 10 W. Prices for the DSP3133L, DSP3107L, and DSP3053L drives are $1285, $1185, and $985, respectively.

Digital Equipment Corp.
334 South St.
Shrewsbury, MA 01545
(508) 841-3111
▶ CIRCLE 543

▼ 1.3-IN. DRIVE DOUBLES IN CAPACITY

Though the Kittyhawk hard-disk drive was the first to fit in a 1.3-in. form factor, it lacked capacity—just 21 Mbytes. Now, with the release of the Kittyhawk II, Hewlett-Packard has doubled the capacity up to 42 Mbytes. In addition, the storage boost comes at nearly half the cost per Mbyte of its predecessor.

The second-generation drive is about the same size and weight as the first version—2 by 1.44 by 0.4 in. and about 1 oz.—but features about 50% higher shock resistance and 25% power savings. The extra capacity comes from increasing the disk's storage density and adding one thin-film read-write head. Although the previous version used two platters, only three of the four media surfaces held data. Now, the fourth surface will store data as well.

The reduced power draw comes from a shorter spin-up time. Most drives take about 5 seconds to reach full speed, while the Kittyhawk II takes about 1 second. The raised shock resistance results from a refined suspension system that contains stiffer actuator arms. This reduces the chance of the heads hitting—and damaging—the media during a shock. Available now in evaluation quantities, the Kittyhawk II sells for about $500.

Hewlett-Packard Co.
Disk Memory Div.
11413 Chinden Blvd.
Boise, ID 83714
▶ CIRCLE 544

▼ TRANSFER DATA USING EXTERNAL PCMCIA DRIVE

As a method of exchanging information between portable and desktop computers, the CardPro universal PC card drive can read and write (when appropriate) to Type-1 and Type-2 PCMCIA-compatible memory and I/O cards. A Type-3 compatible drive should be released later in the year. The CardPro gets configured as an extra drive in a system and uses familiar DOS commands. It connects through a parallel and contains a transparent pass-through port for printing.

Another feature of the CardPro drive is its ability to read and write to PCMCIA-compatible flash-memory cards. Flash memory requires a unique write sequence which differs from that of magnetic memory. The "FlaSH" developed by Microsoft Corp. and licensed by Data I/O automatically manages the process of writing to flash memory from the DOS environment. With an optional developer's kit, users can edit both common and attribute memory, edit tuples in both block and logical form, and create and transfer card-image data. It also contains diagnostic and card-information utilities. Available now, the CardPro sells for $450.

Data I/O Corp.
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073
(206) 881-6444
▶ CIRCLE 545

▼ RADIO MODEM BOARDS SEND DATA TWO MILES

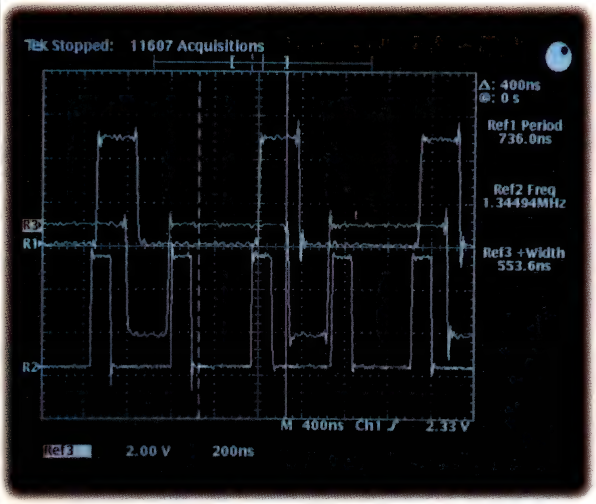
A radio modem, called the System 200, eliminates many interconnecting cables within PCs and peripherals. The two-board set sends serial data with an output level ranging from 1 mW to 2 W. At 2 W, the line-of-sight connectivity can be 2 miles. One board is a digital transmitter-receiver; the other is a high-performance modem. The two are linked by a flex cable that carries only low-frequency signals and direct current. The power requirement is 7.5 V, supplied through the RS-232 interface connector or by NiCD batteries on the modem board. The bundled software handles up to 48 terminal nodes. In quantities of 1000, the System 200 sells for $465.

Monicor Electronic Corp.
2964 NW 60th St.
Ft. Lauderdale, FL 33309
(305) 979-1907
▶ CIRCLE 546

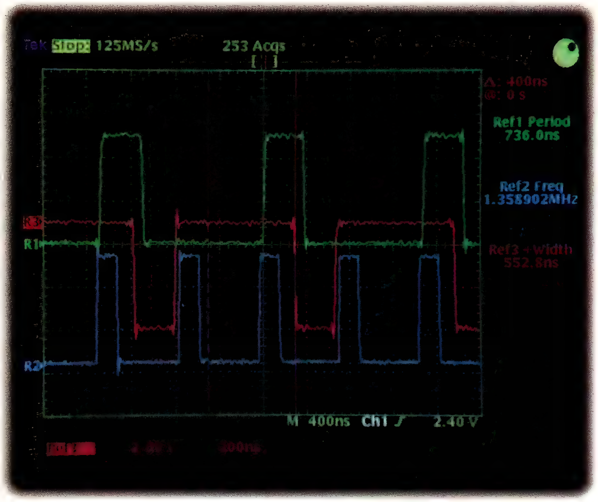
▼ INSERT VME BOARDS WITHOUT POWERING DOWN

Users of VME systems can insert and remove individual boards within a VME rack without interrupting the power to the system using the Live Insertion Module (LIM). The module is installed in a standard VME rack between the backplane and a standard 6U VME board. When the rack is powered on, the module either powers up a board that's present or links the daisy-chain signals to the next slot. In the board-removal process, the LIM requests the bus to ensure that the sequence doesn't interrupt an operation. It then isolates the board, releases the bus, and powers down the slot.

Mupac Corp.
10 Mupac Dr.
Brockton, MA 02401
(508) 588-6110
▶ CIRCLE 547



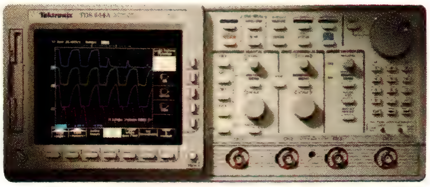
HOW QUICKLY CAN YOU FIND YOUR PULSE?



With the new TDS color digitizing oscilloscopes and their dazzling displays, you can find a specific pulse in about a heartbeat.

Even if the little guy is badly outnumbered.

And aside from providing 500 MHz bandwidth and a graphical user interface, you can get a TDS color scope with sampling rates to 2 GS a second across four channels.



Plus up to 50,000 point record length and measurement accuracy to 100 ps.

These color scopes also come with a high-resolution monitor, a DOS compatible floppy drive so you can store personal waveforms and setups on a PC, and a VGA output that allows you to display your work on a larger monitor.

What's more, an optional video trigger lets you pinpoint any color field, and you can specify the trigger for any HDTV format.

Now if all that gets your blood pumping, you better sit down. Because you can get a color TDS for about the same price as any high-bandwidth four-channel monochrome scope. You know, monochrome. Like the one up there on the left.

If you're tired of working in white-out conditions, call us toll free at 1-800-426-2200, ext. 162 and ask about the TDS 544A and 644A.

We may not be able to help you find your pulse over the phone, but what we have to say should quicken it.

Tektronix

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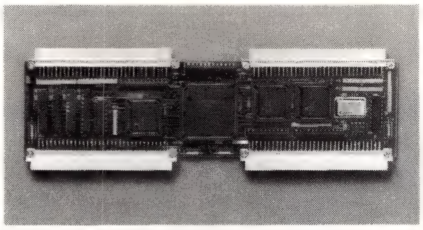
CIRCLE 210 FOR U.S. RESPONSE **CIRCLE 211 FOR RESPONSE OUTSIDE THE U.S.**

▼ INSTALL A VME BOARD IN A MULTIBUS II CHASSIS



By taking advantage of the LBX.VME board, a 6U VME board can be installed in a Multibus II chassis. The host processor in the Multibus II system sends data through the LBXVME board, over its iLBX bus. Then the data is transferred to the attached VME board. Applications for this configuration include using VME reflective memory on a Multibus II simulator or driving VME peripherals from a Multibus II system. The LBXVME performs all data and control translation between the installed VME device and the Multibus II system. The seven VME interrupts are mapped into the sole LBX interrupt. The LBXVME board sells for $2395.

Applied Data Sciences Inc.
P.O. Box 814209
Dallas, TX 75381
(214) 243-0113
▶ CIRCLE 548

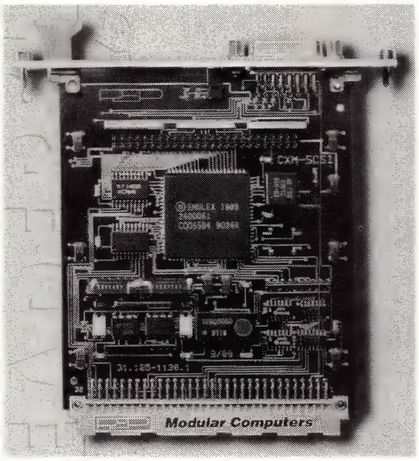
▼ DATABASE MAXIMIZES WINDOWS FEATURES

Relational databases that run under the Windows operating system are just starting to emerge. FoxPro, a traditional DOS-based database, has now been ported over to Windows. The 32-bit application takes advantage of all Windows' benefits, including the familiar user interface. Users running applications such as Excel or Word for Windows can integrate the data from those applications using Windows' dynamic data exchange. As a result, complex objects like spreadsheet charts, photos, and video can be stored in a database using the object-linking and -embedding feature. FoxPro version 2.5 is available now for $495. Users of earlier FoxPro versions can upgrade for a reduced fee.

Microsoft Corp.
One Microsoft Way
Redmond, WA 98052
(206) 882-8080
▶ CIRCLE 549

▼ VME MODULE PERFORMS SCSI FUNCTIONS

The CXM-SCSI is a VMEbus-compatible SCSI interface mezzanine module that takes up less than one-third the area of a full-height VME board. The board offers high performance to SCSI-1 and SCSI-2 peripherals, such as disk drives, CD-ROMs, tape-backup units, and scanners. It extends the control, address, data lines, and asynchronous behavior of an underlying microprocessor onto a module. The CXM-SCSI is built with the NCR 53C94 single-chip SCSI controller (or Emulex equivalent). As a result, it supplies ANSI-compatible tagged-queuing functions. Also included is a high-speed serial port. Available now, the board sells for $290 in small quantities.



PEP Modular Computers
750 Holiday Dr., Bldg. 9
Pittsburgh, PA 15220
(412) 921-3322
▶ CIRCLE 550

▼ DEVELOP 680X0 APPLICATIONS ON A PC

Version 1.1 of the PDOS/MS-DOS Backplane Communications Services (BCS) lets designers use 80X86-based PCs to develop real-time PDOS applications for Motorola 680X0 processors. The BCS combines a high-performance, multitasking, source-level debugging environment with a low-cost MS-DOS interface and popular user applications. By giving users their familiar low-cost front-end, 680X0 code becomes easier to develop. It also lets the host DOS-based CPU reside in the same VME backplane, or it can be connected through a VMEbus adapter. The BCS is included as part of the PDOS Full Spectrum development kit, which sells for $3000.

Eyring Corp.
1455 West 820 North
Provo, UT 84601
(801) 375-2434
▶ CIRCLE 551

▼ MEZZANINE MODULE IMPLEMENTS SUPER VGA

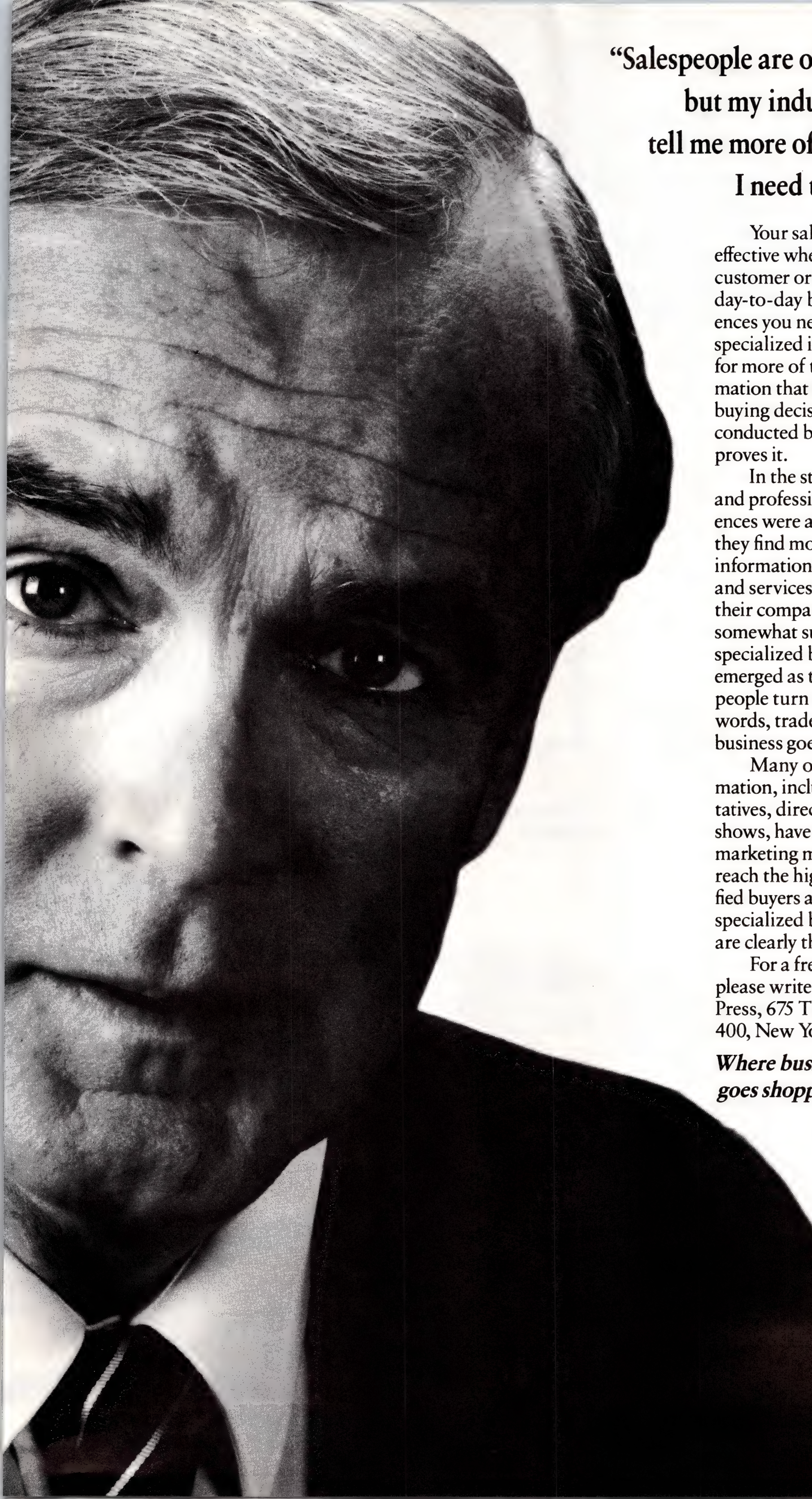
IndustryPack modules are mezzanine boards that fit into larger base boards for customization purposes. The IP-SVGA is a module that performs the functions of a Super VGA board, including the ability to run Microware's Rave and Gespac's G-Windows, which are two graphical user interfaces for industrial automation. Built with Cirrus Logic's CL-GD5422 controller, the module supports either 256 or 512 kbytes of video memory. Because the data is passed across the mezzanine bus rather than the conventional backplane, the potential bottleneck is avoided. The 256-kbyte version of the IP-SVGA sells for $255, while the 512-kbyte models costs $395.

GreenSpring Computers Inc.
1024 O'Brien Dr.
Menlo Park, CA 94025
(415) 327-1200
▶ CIRCLE 552

▼ EXTEND FAST SCSI CABLE TO 102 FT.

Using the SD10 SCSI single and differential converter, a total cable length of 102 ft. can be employed. When converting from single to differential SCSI, 20 ft. can be used on the single-ended side and 82 ft. on the differential side. In a single-ended application, two SD10s can be used to extend the cables over 200 ft. Data is transferred over the cable at a rate of 10 Mbytes/s (fast SCSI), and no hardware or software modifications are necessary. The converter, a standalone external box with its own power supply, sells for $475. A internal version, the model SD11, can be mounted inside a system or peripheral. The internal-version model SD11 is priced at $285.

Paralan Corp.
7171 Ronson Rd.
San Diego, CA 92111
(619) 560-7266
▶ CIRCLE 553



“Salespeople are often helpful, but my industry publications tell me more of what I need to know.”

Your salespeople can be effective when they get to see a customer or prospect. But, on a day-to-day basis, the buying influences you need to reach turn to specialized industry publications for more of the important information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, proves it.

In the study, 9,823 business and professional buying influences were asked what sources they find most useful in providing information about the products and services they purchase for their companies. The results were somewhat surprising. Overall, specialized business publications emerged as the source business people turn to first. In other words, trade magazines are where business goes shopping.

Many other sources of information, including sales representatives, direct mail and trade shows, have their place in the total marketing mix. But if you want to reach the highest number of qualified buyers at the lowest cost, specialized business publications are clearly the best choice.

For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

Where business goes shopping. **ABP**

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European Division: Barchon, Belgium
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CIRCLE 234

NOVEL IC MERGES SRAM AND FIFO FUNCTIONS

BY COMBINING THE FEATURES OF AN SRAM AND A FIFO BUFFER, A SEQUENTIAL-ACCESS RAM CAN MATCH SUBSYSTEM DATA RATES.

DAVE BURSKY

Specialty memories such as dual-port RAMs and first-in/first-out (FIFO) buffers offer designers several advantages. For instance, each type of memory assists systems that require communication interfaces between independent subsystems, adjusts data rates between low- and high-speed subsystems, or just buffers moderate amounts of data. Very often, systems require both types of memories working in tandem to solve interface or buffering problems. However, that results in a multipackage solution, including some additional control logic.

By combining the functionality of a bidirectional synchronous FIFO buffer on one port and the random-access capability of a static RAM on the other, designers at Integrated Device Technology created a new system component dubbed the sequential-access RAM (SARAM). The new concept is embodied in the company's model IDT70825 memory IC.

The IDT70825, which crams in 128 kbits of storage, is organized as 8 kwords by 16 bits. It allows memory accesses in as little as 25 ns on either its 16-bit asynchronous random-access port or its synchronous 16-bit FIFO port.

When running at top speed with both ports active, the chip consumes between 1.5 and 1.8 W of power. When idling, though, the SARAM's power drain drops to between 25 and 75 mW. A 2-V data-retention mode trims the power drain to about 8 mW. Because of the chip's high speed and moderate depth of the memory, it can be applied in telecommunications, internetworking, disk arrays, graphics and image processing, I/O control, and many other application areas.

The dual structure of the memory is somewhat reminiscent of the concept implemented in video RAMs (VRAMs), which also have a random-access port on one side and a 4- or 8-bit serial-transfer port on the other. However, the SARAM has several features not available on VRAMs or FIFO memories. Those features enhance the SARAM's functionality and let it handle tasks that even dual-port RAMs used with standard FIFOs can't tackle.

A DIFFERENT SRAM

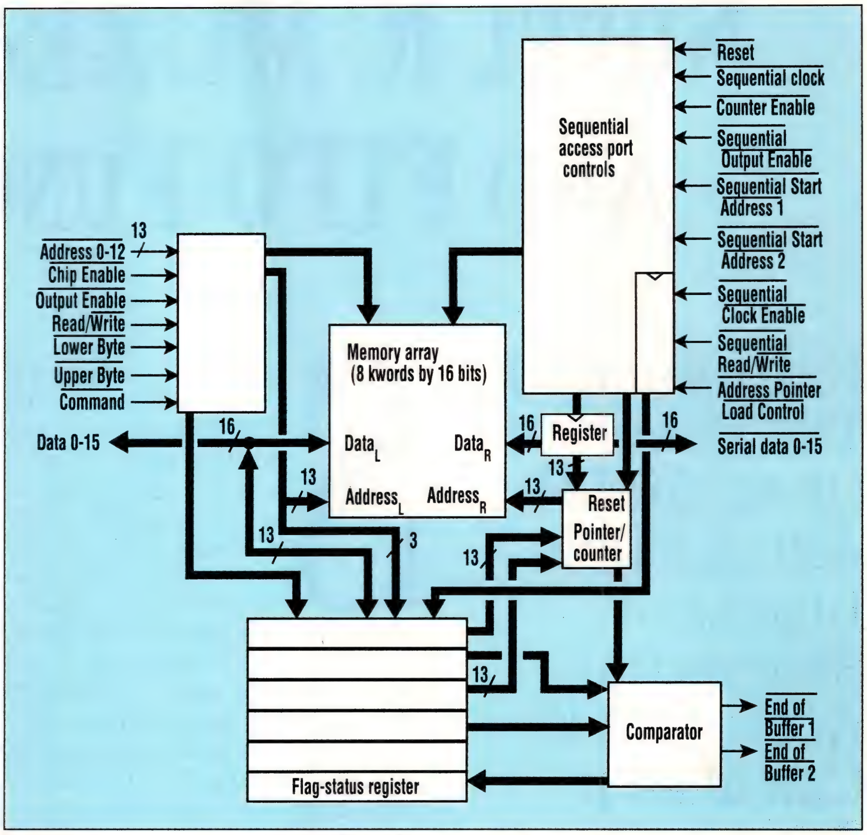
At the heart of the memory lies the 8-kword-by-16-bit dual-port storage array. It's surrounded by the port control logic, various pointer registers, and the pointer counter and comparator *(see the figure)*. The RAM port acts like a standard SRAM port with two exceptions. First, the port has separate upper- and lower-byte control for reading or writing data in byte-sized sections or word-size increments. Secondly, the port contains a command pin so that the system can load various control words into the pointer and control registers.

The other port contains the logic that turns the RAM array into a clocked bidirectional FIFO buffer—the address pointer and comparator, various registers to hold the starting and ending addresses for the address pointer, and both a flow-control register and a flag-status register. There are two sets of starting and ending address registers. Those register pairs allow users to set up two independent buffer areas or one contiguous buffer region, either of which can span the entire address range of the RAM array.

Both the RAM and FIFO ports can simultaneously be active, with dual reads, dual writes, or reads and writes (as long as the write isn't to the same address as the read). As a result, both sides of the system can run at top speeds, minimizing the impact of slow buses or peripherals. For instance, the system can perform sequential 16-bit writes to the FIFO port, and read out the data in "random" sequence, or perform sequential reads from the FIFO port while the other side of the system delivers "random" writes to the RAM port. In addition, simultaneous reads can take place over both ports, and simultaneous writes can occur on each port (again, assuming the write operations are to different locations).

External arbitration logic is needed for the two possible conflicting situations—simultaneous writes to the same location, and a simultaneous write into and read from the same location. Most of the time, software can prevent such situations from occurring. But as a precaution, a programmable-logic-device (PLD) can be used to implement the conflict-resolution logic.

The PLD combined with the 80-lead thin, quad-sided flat package (14 by 14 mm) provides a compact, low-chip-count solution. The SARAMs can also be cascaded to expand the word width or depth.



THE DUAL-PORTED MEMORY ARRAY, surrounded by all of the port-control logic, allows the RAM port to randomly access all of the address locations. At the same time, the bidirectional FIFO port enables every data location to be read out or written to sequentially, depending on the addresses loaded into the pointer-control registers. The RAM port acts like a standard SRAM port with two exceptions. It has separate upper- and lower-byte control for reading or writing data in byte-sized sections or word-size increments, and a command pin for system loading of control words into pointer and control registers.

A SINGLE SET

The two pairs of address-pointer registers provide starting and ending addresses for the two independent buffer-address spaces. The 13-bit registers allow the entire depth of the memory array to be covered with a single set of starting and ending addresses. Thus, by loading the proper addresses, the user can set up either two independent, non-overlapping spaces; two independent overlapping spaces; two consecutive spaces; or effectively, one contiguous address space.

Address-space mapping is controlled by the Flow Control Register and two Flag-Status bits in the Flag-Status Register. The Flow Control Register has two 2-bit fields, one for each buffer, that control the chaining capability of the two buffers. A fifth bit, the Counter Release bit, is also used with the fields to restart the counter after the first buffer reaches its terminal count.

Each buffer also has a corresponding flag bit in the Flag Register that's set when the counter reaches the end-of-buffer (EOB) value. Each buffer can operate in any of four modes. The four modes are a buffer-chaining mode, a stop-after-terminal count mode, a linear mode, and a mask mode.

In the buffer-chaining approach, when the terminal count of one buffer is reached, the second buffer picks up and continues the count. In the stop-after-terminal count mode, after the first buffer reaches its count, access to the locations stops until the Counter Release bit is reset to restart the counter for the second buffer.

As for the linear mode, when the first buffer hits its terminal count, the EOB signal is asserted, but the address counter keeps incrementing. Lastly, in the mask mode, the Flag bit is set when the first buffer hits its terminal count, but the EOB signal isn't asserted. However, the EOB flag-status bit is set internally. These options give designers a number of capabilities when implementing systems with either software or hardware control.☐

PRICE AND AVAILABILITY

The IDT70825 comes in both a standard version and a lower-power option for power-critical applications. In 1000-unit lots, SARAM prices start at $49.35 each in the 80-lead thin quad flat pack (TQFP) package. An 84-lead pin-grid-array (PGA) package is also available. Samples are immediately available. **CIRCLE 520**

HOW VALUABLE?	CIRCLE
HIGHLY	576
MODERATELY	577
SLIGHTLY	578

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Asked whether they are satisfied "with the way things are going in the United States," 49% of Americans said "no."

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"No," despite the fact that 31% of families now have incomes exceeding $50,000, up from 19% in 1970.

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We think the problem is summed up in another statistic. The golden promise of a service-producing economy has begun to tarnish. Productivity in services grew only .8% per year during the last decade. And services today employ 70% of the total work force.

By contrast, manufacturing, which increased productivity by 3.9%, employs only 16% of the work force.

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PUT THE US BACK IN BUSINESS:
CREATING WEALTH

CAE FRONT END MESHES TOOLS AND DATABASE

Active-CAD 1.0 from Aldec is a Windows 3.1-based CAE front-end tool that meshes schematic capture, background logic simulation, and a project-database-management system. Project management allows for smooth reuse of old design data, including schematic sections, test vectors, and Jedec and hex files. These existing data resources are linked together with new design data in one database, ensuring project integrity and improved productivity.

Because it looks and acts like any other Windows software, Active-CAD is easy to learn and use. All operations are intuitive and compilation-free. For example, any device drawn on the screen instantly becomes active as it's connected to an active signal line. The Active-CAD schematic essentially behaves like a combination hardware breadboard, signal generator, and logic analyzer.

Active-CAD analyzes each schematic entry and provides instant design feedback as the circuit is drawn. For example, wiring is checked for electrical rules compliance and device operation is verified for bus conflicts and timing violations. In addition, users need not get involved with the details of individual device operation because the electronic breadboard tracks the timing and loading effects on each device operation. Should any problems occur, users are alerted and given a table of replacement parts.

Innovative features free users from tedious design tasks. The design milestones feature lets users restart a design at any past simulation cycle. Also, automatic design correction analysis compares simulation and underscores the circuit improvements due to design or test-vector changes.

Active-CAD 1.0 includes schematic capture, TTL-components library, and a simulator with 10-ps timing resolution. The software, which will ship at the end of this month, runs on 80386- and 80486-based PCs under Windows 3.1. Pricing ranges from $995 to $6495.

Automated Logic Design Co. Inc., *3525 Old Conejo Rd. #111, Newbury Park, CA 91320; (805) 499-6867.* **CIRCLE 601**

■ *LISA MALINIAK*

UNIVERSAL SCHEMATIC TOOL RUNS IN WINDOWS

SCHEMAx is a Windows-based universal schematic-capture program from Omation that acts as a front end for many of the popular pc-board layout systems. The schematic software accepts a number of net-list inputs. It also supports forward and back annotation with Omation's pc-board tools, as well as those from Accel Technologies, OrCAD, Pads Software, P-CAD, and others. SCHEMAx accepts drawing files from all older version of the DOS-based SCHEMA packages. However, the Windows-based software has many new features not found in the older DOS versions. For example, all parts and text can be mirrored, scaled, rotated, and presented in users' choice of colors. Other features include hierarchical structure, more than 15,000 library parts, a design-rule checker, and an optional autorouter. The autorouter module routes the schematic, cleans up signal lines after a part or region movement, and connects pins on schematics imported from other systems. SCHEMAx, which is available now, runs on a PC under Windows. It costs $595. The optional autorouter goes for $149.

Omation Inc., 801 Presidential Dr., Richardson, TX 75081; (800) 553-9119. **CIRCLE 602**

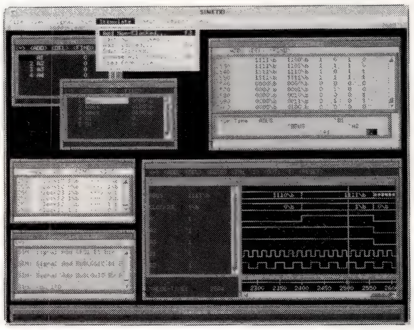
LOW-COST WINDOWS TOOL MODELS IN 3D

Autodesk 3D Concept for Windows is conceptual design software that runs under the Microsoft Windows interface and costs just $249. The Autodesk package extends the visually-oriented Windows interface concepts to CAD and 3D modeling. On-screen visual tools aid new users in mastering complex drawing techniques quickly. For instance, users can change the orientation of an object or set of objects by manipulating a color-coded icon called the rotation cube. Another interface feature, the visible ground plane, establishes the 3D frame of reference so users can identify the top or bottom of a model at a glance. With the align-to-plane function, users simply click on the desired surface to draw and edit objects on that plane. Also, users have a choice of shading speed depending on the size of their file. Graphic on-line help and tutorials speeds the learning process. While it's easy to use, the package also incorporates powerful CAD and 3D modeling capabilities, such as light-source shading, hidden-line removal, and view changing. Autodesk 3D Concept requires a PC running Windows 3.0 or 3.1.

Autodesk Retail Products, 11911 N. Creek Pkwy. South, Bothell, WA 98011; (800) 228-3601. **CIRCLE 603**

SIMULATOR UPGRADE ADDS VHDL SUPPORT

Version 2.0 of the EPS Simetri logic simulator for Sun workstations and PCs adds support for VHDL and Microsoft Windows, respectively. In addition, this new version has features that enhance productivity, particularly for designs over 300,000 gates. EPS claims that their simulator runs up to 10 times faster than current logic simulators. Simetri also has a compact data structure that uses as few as 50 bytes per primitive, giving it the capacity to simulate well over 500,000 gates on a 32-Mbytes desktop workstation without paging to disk. A graphical user interface offers various methods of simulator operation, including a mouse-driven menu, function keys, or a command line. The workstation version of Simetri has optional VHDL support so users can simulate mixed VHDL and gate-level descriptions in the same simulation run. Simetri Version 2.0 will ship by the end of the second quarter.



Evaluations Per Second Inc., 100 Fifth Ave., First Floor, Waltham, MA 02154; (617) 487-9959. **CIRCLE 604**

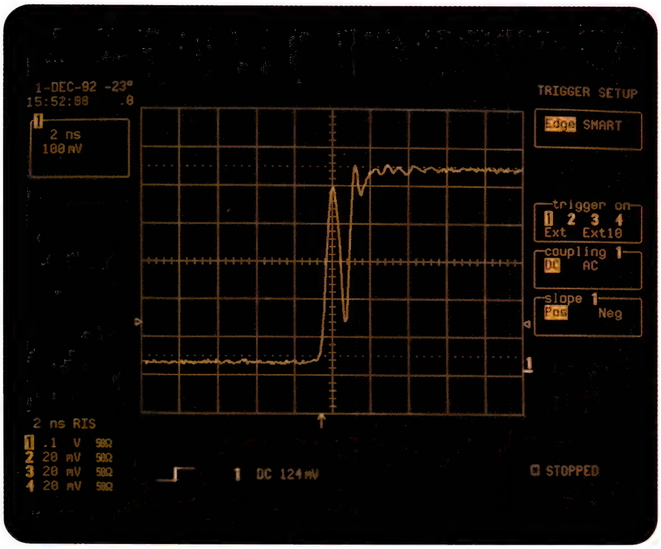
DESIGN PACKAGE BUILDS REAL-TIME SYSTEMS

A design package that meshes software and hardware tools helps engineers design, simulate, and implement real-time control and embedded systems. The product is based on The MathWorks' design software, and hardware tools from dSpace Inc. Software products include Matlab for numeric computation, Simulink for modeling and analysis, and application-specific toolboxes. The dSpace hardware offerings include plug-in boards for PCs, expansion boxes with bus interfaces, and Ethernet-compatible expansion boxes for lab or in-vehicle use. All hardware is based on DSP technology. The integrated software-hardware product is available now on the Sun workstation for $30,000. Other platforms will be supported later this year.

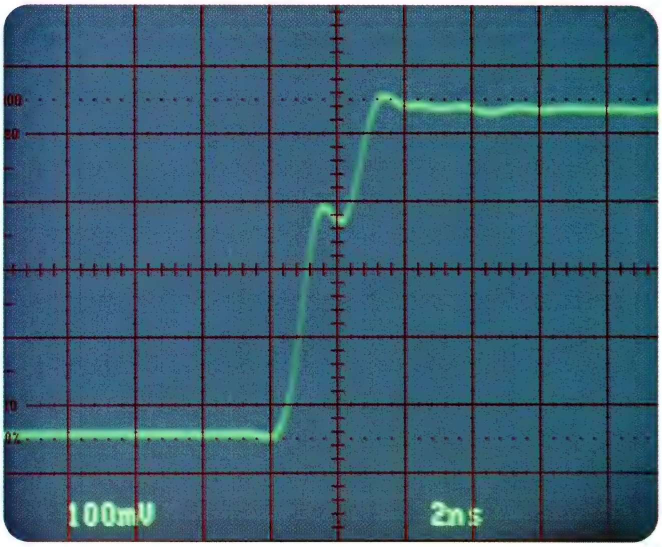
The MathWorks Inc., Cochituate Pl., 24 Prime Park Way, Natick, MA 01760; (508) 653-1415. **CIRCLE 605**

Debugging Fast Logic...

...with a LeCroy 1 GHz scope.



...with a 350 MHz scope.



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Circle 192 For Product Information

TOUCH TERMINALS HOUSE STORAGE, NETWORKING, HIGH-END PROCESSORS

Flat-panel touch-screen displays are becoming popular in commercial, industrial, and public-access markets. The Ergo family of high-resolution, color touch terminals, which can house storage subsystems, networking, or high-end processors, is suitable for those types of environments.

The touch surface, active-matrix display, and logic board are packaged in an environmentally sealed enclosure that can be mounted in or on panels, walls, kiosks, and consoles; it can be suspended from boom mounts also. The touch surface extends above, beside, and below the display itself. As a result, printed screen overlays can be customized to display permanent touch zones, an OEM's logo, or other application information.

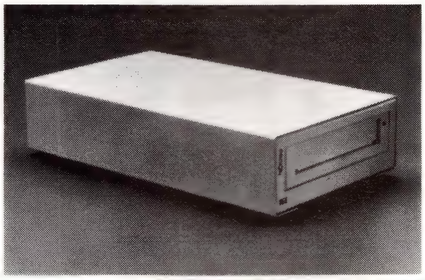
Three different versions of the Ergo family are available. One comes with built-in software for real-time supervisory control with interactive graphics. The second is a full-function X-Windows terminal. And the third is a direct upgrade for an earlier generation of terminals. Prices start at $4500.

***Dynapro Technologies Inc.**, 800 Carleton Ct., Annacis Island, New Westminster, British Columbia, Canada V3M 6L3; (604) 521-3962.* **CIRCLE 606**

■ *RICHARD NASS*

PORTABLE BACKUP DEVICE IS JUST 1.5 IN. HIGH

The Model 250P portable data-storage backup unit at 1.5 in. high and less than 2 lbs, has a capacity of 250 Mbytes of compressed data, accessed through a parallel port. The quarter-inch cartridge (QIC) unit also features a transfer rate of 150 kbytes/s. An additional port on the device's cable makes possible simultaneous printer operation. The 250P sells for $549. An internal version, the 250I, is also available.



Storage Devices Inc., 6800 Orangethorpe Ave., Buena Park, CA 90620; (714) 562-5500. **CIRCLE 607**

HARD DRIVE UPS CAPACITY

The 7245 is a 1-in. high, 3.5-in. form factor drive that holds 245 Mbytes of formatted data. Available with either a SCSI or an AT interface, the drive boasts an average seek time of 15 ms, with a track-to-track seek time of 3 ms. It is built with the same architecture as the previous generation, the 7212, just with a higher capacity. The electronics housed within the drive are mounted on one side of a pc board using surface-mount technology. Evaluation units with either interface are available now for $395.

Maxtor Corp., 211 River Oaks Pkwy., San Jose, CA 95134; (408) 432-1700. **CIRCLE 608**

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CIRCLE 100 FOR U.S. RESPONSE
CIRCLE 101 FOR RESPONSE OUTSIDE THE U.S.

RAMDAC ADDS VIDEO PORT

By loading video and graphics asynchronously through separate ports, Brooktree's Bt885 Video CacheDAC provides optimal partitioning of the video subsystem and eliminates the need for a graphics subsystem on video add-in cards.

Besides the separate video path, the device integrates standard RAMDAC functions, a YCrCb-to-RGB color space converter, and horizontal scaler. It can maintain the 135-MHz throughput required for a 1280-by-1024-pixel display and supports VRAM and DRAM-based video subsystems. The horizontal scaler allows the video image to be stored in its native resolution and scaled on chip before being displayed, cutting memory costs and bandwidth requirements.

The chip is another building block in Brooktree's proposed VideoCache architecture for 80486 and 80586-based PCs. Other chips include the all-digital Bt812 for video synchronization and the Bt858 video encoder.

When used in video systems dependent on software compression, the Bt885 enhances performance by off loading the processor of color conversion and scaling functions.

The Bt885's hardware interface, a 64-bit pixel port, can be subdivided to support several combinations of graphics and video multiplexing modes. It can operate with video decompression and video processor chips using programmable interpolation for 4:2:2, 2:1:1, and 1:0.5:0.5 formats so video mixes with graphics at the same rate. Video data can be displayed in 15-, 16- and 24-bit RGB formats. Priced at $42.65 in hundreds, will be available in June.

Brooktree Corp., 9950 Barnes Canyon Road, San Diego, CA 92121; (619) 457-7580. **CIRCLE 609**

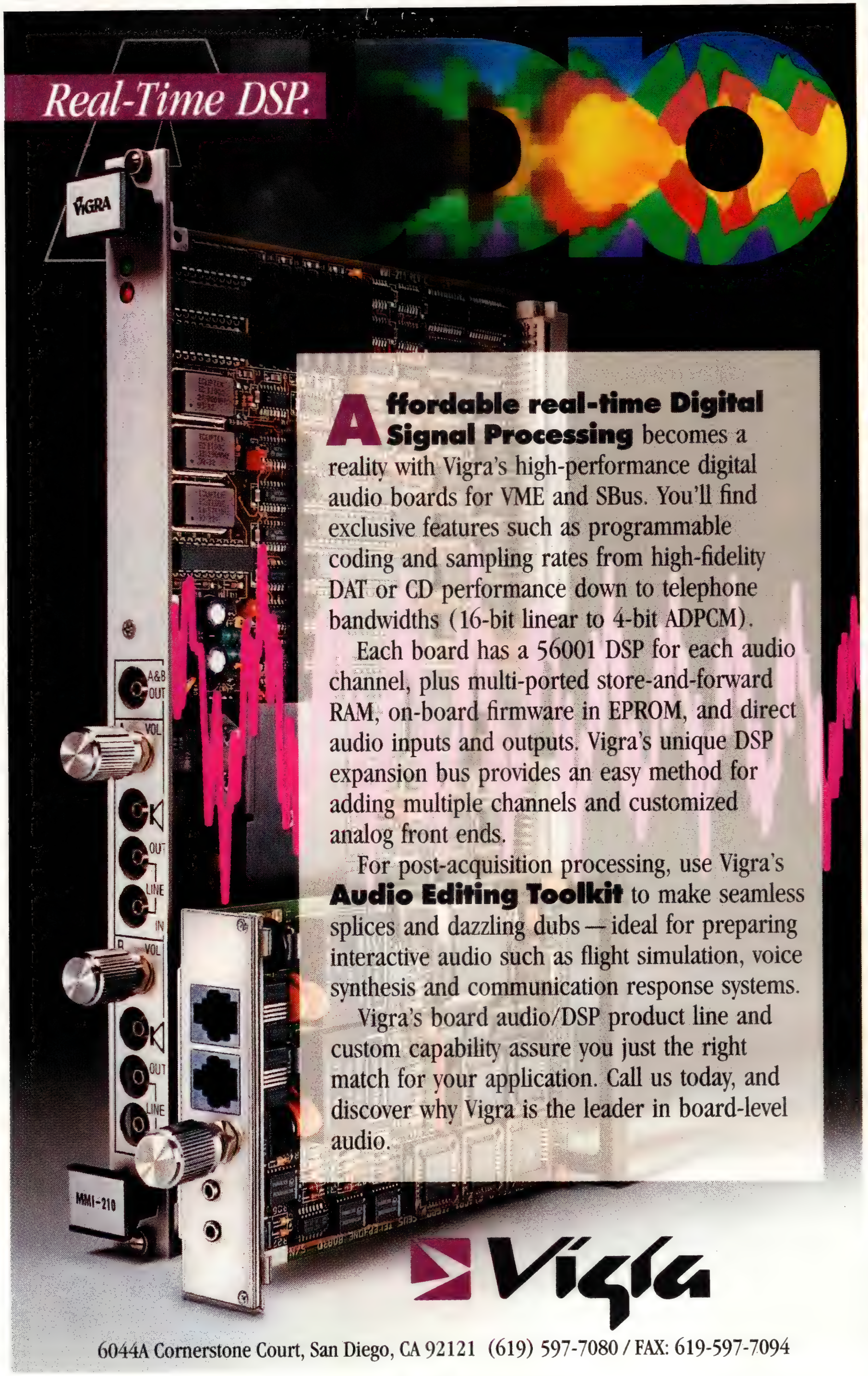
■ *JACK SHANDLE*

GAAS GATE ARRAYS CHALLENGE BICMOS COST

Offering two to three times the performance of biCMOS at a price competitive with silicon gate arrays, the Viper family of digital GaAs gate arrays helps designers build higher performance systems. The family consists of three base arrays—the VGLC2K, 10K and 15K, which provide 1500, 7000, and 13,000 usable gates, respectively. Typical loaded gate delay for a 2-input NOR is just 130 ps—about half to one-third that of a loaded biCMOS gate. Power dissipation of the gate is about 0.7 mW, similar to the power consumed by a biCMOS gates. The chips suit operations between 75 and 200 MHz and are ideal for peripheral, communications, imaging, graphics, and instrumentation. The VGLC2K has 36 I/O pins and comes in a 44-lead plastic leaded chip carrier; the 10K has 71 I/O pins and comes in a 100-lead PQFP; and the 15K provides 140 signal lines and comes in a 160 lead PQFP. All I/O pins can be TTL, ECL or mixed ECL/TTL. The packages are thermally enhanced to efficiently dissipate the heat caused by the high-speed operation. Non-recurring engineering charges start at $25,000 and production chip pricing starts at less than half a cent per gate.

Vitesse Semiconductor Corp., 741 Calle Plano, Camarillo, CA 93012; Brett Butler, (805) 388-7408.

CIRCLE 610



Affordable real-time Digital Signal Processing becomes a reality with Vigra's high-performance digital audio boards for VME and SBus. You'll find exclusive features such as programmable coding and sampling rates from high-fidelity DAT or CD performance down to telephone bandwidths (16-bit linear to 4-bit ADPCM).

Each board has a 56001 DSP for each audio channel, plus multi-ported store-and-forward RAM, on-board firmware in EPROM, and direct audio inputs and outputs. Vigra's unique DSP expansion bus provides an easy method for adding multiple channels and customized analog front ends.

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CIRCLE 230 FOR U.S. RESPONSE
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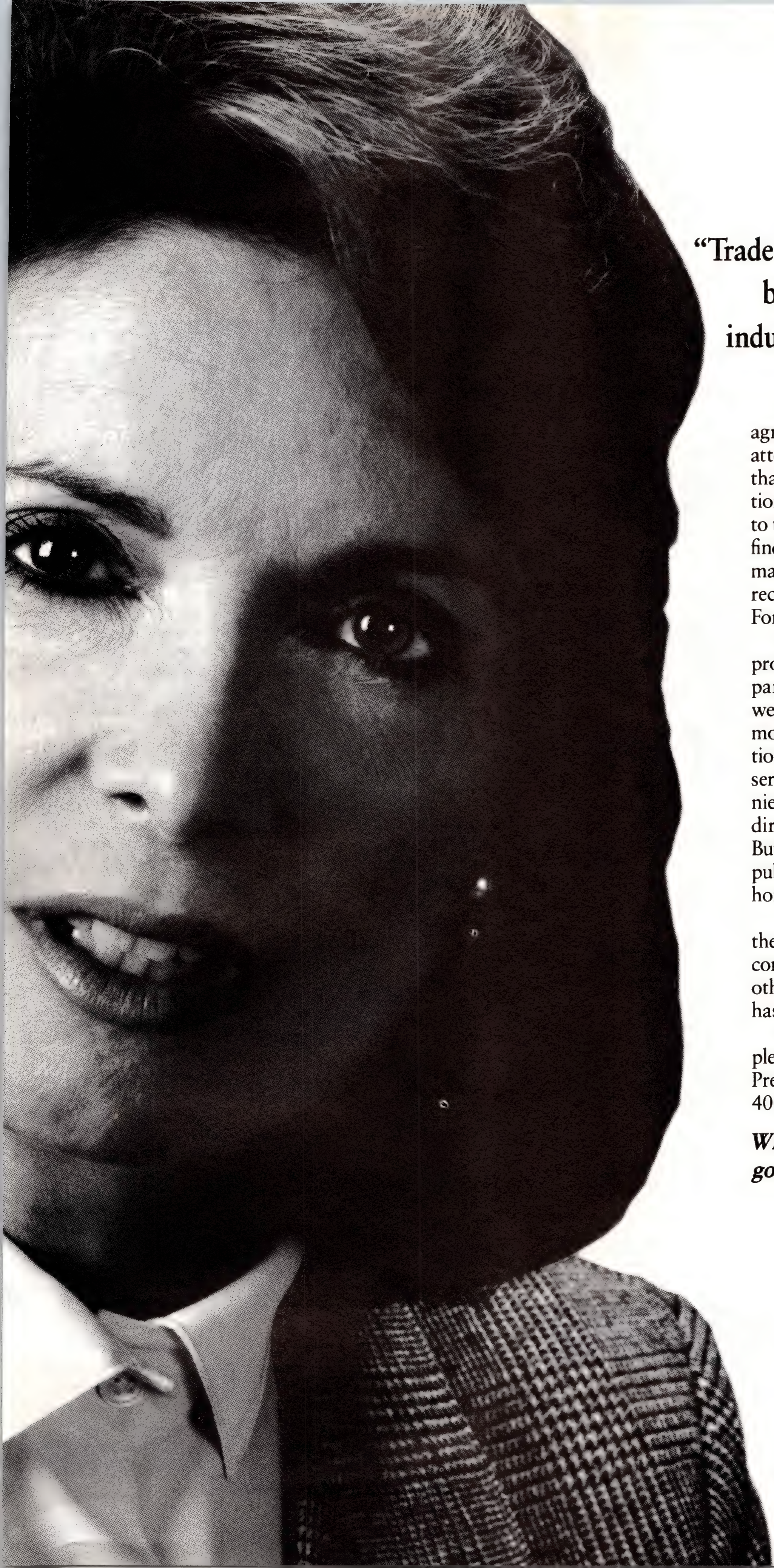

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Almost 10,000 business and professional decision makers participated in the study. They were asked what sources they find most useful in providing information about the products and services they buy for their companies. Trade shows, salespeople and direct mail were all well regarded. But overall, specialized business publications clearly took top honors.

Trade magazines are also at the top of the list when you consider cost per contact. No other medium is more efficient. Or has more credibility.

For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

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TOOL TARGETS REAL-TIME DEVELOPMENT

FasTrak, a development environment for the OS-9 real-time operating system, has an X Windows/Motif user interface and runs on Unix cross-development hosts. Communication between the host and OS-9 target is conducted by either Ethernet TCP/IP or a serial link. FasTrak can also be self-hosted on OS-9/680X0 target systems.

Fastrak is aimed at the implementation stage of project development: source code creation and revision, code generation, source-level debugging, system and application profiling, and software version control. The environment has automated facilities for editing and repairing C programs, an automated push-button utility for generating "makefiles," and context-sensitive online help. FasTrak's source code control systems and project-context files, which save working parameters for each project, help ensure consistency and coordination among multiple team members.

The environment is made up of the FasTrak Workbench, Test Editor Tool, Makefile Editor Tool, FastFix Debugger, and Target Monitor. From the Workbench, users can manipulate project files and directories, set user preferences, and run-time options, launch other FasTrak tools, access the version-control system, and automatically build and execute programs.

FasTrak runs under Unix on Sun/3, Sun/4, SparcStation, and HP9000 workstations. With the Ultra C compiler, FasTrak goes for $14,500 for up to five networked workstations. FasTrak for resident OS-9 development is $3,750 per system. DOS/Windows versions will be available in July.

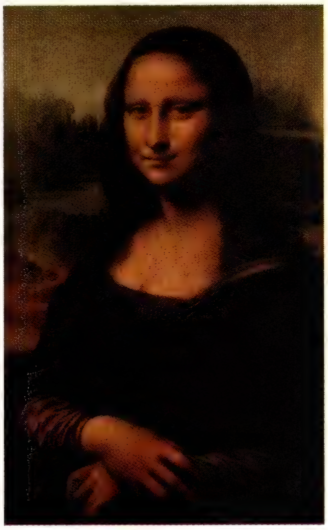
Microware Systems Corp., 1900 N. W. 114th St., Des Moines, IA 50325; (515) 224-1929; fax (515) 224-1352. **CIRCLE 611**

■ *SHERRIE VAN TYLE*

TOOLS ADD NEAR FAULT TOLERANCE

Targeted at midrange systems, the LifeKeeper FRS offers detection and recovery from failures in systems, applications, and components. The product consists of a set of software, services, and tools for near fault tolerance, a capability typically seen in high-end systems. The package is suitable for such applications as telecommunications, financial, government, and retail and commercial industries. A scalable availability feature limits computer outages by pairing systems. A multidirectional switchover automatically kicks in, without any user intervention. LifeKeeper FRS will be available in the second quarter. Prices range from $6000 to $30,000, depending on availability, performance, and service.

NCR Corp., 1700 S. Patterson Blvd., Dayton, OH 45479; (800) 225-5627. **CIRCLE 612**



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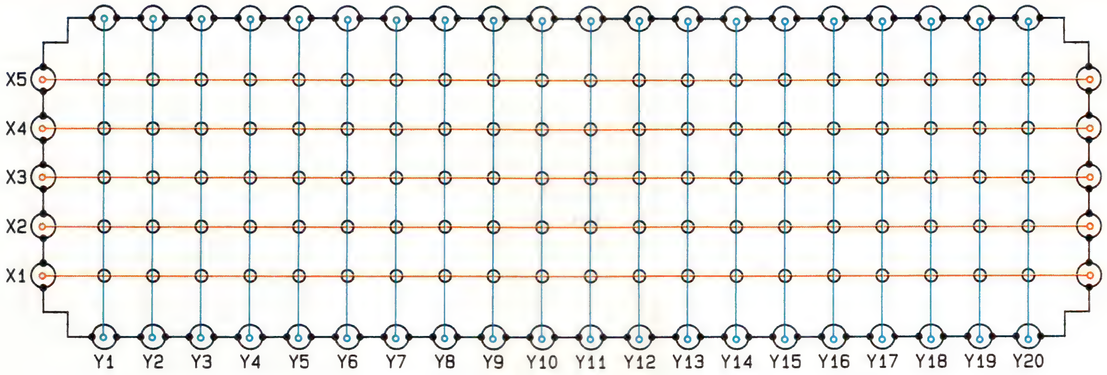

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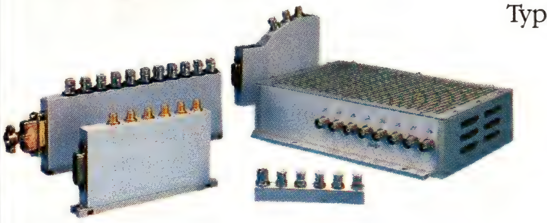

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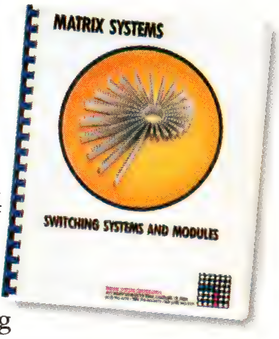

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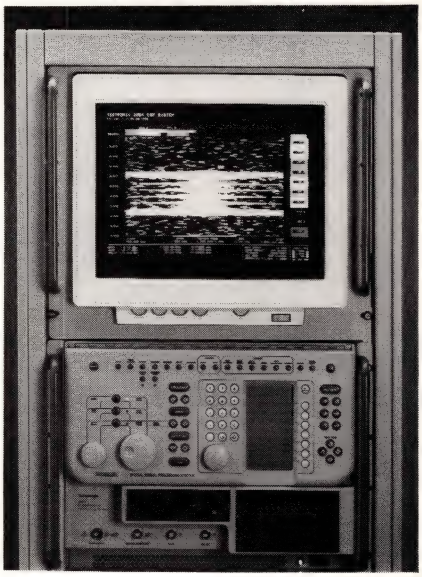
CIRCLE 144 FOR U.S. RESPONSE CIRCLE 145 FOR RESPONSE OUTSIDE THE U.S.

ANALYZER OFFERS 12.5 μS SPECTRAL FRAME UPDATES

A unique bank-of-filters analyzer and a new processing method allow the 3054 DSP System to deliver real-time spectrum analysis at spectral frame update rates as fast as 12.5 μs. Also, new memory processing and data- compression techniques expand stored capture times to a range of 0.8 s to more than 26,000 s.

The system's digitally implemented bank-of-filters ensures a true and accurate measurement of spectral power with high spectral resolution. Users can select transform sizes from 32 to 1024 bins (26 to 801 displayable) to allow flexibility in time and frequency resolution. A tunable center frequency allows users to view any frequency within the dc to 10-MHz range at reduced spans (100 Hz to 10 MHz) and higher resolutions.



Individual spectral frames can be displayed as power or phase versus frequency. Or frames can be viewed in a time-frequency series (spectrogram) with color-coded amplitude. The system is fully programmable via a built-in C compiler and Unix operating system. A split-screen function allows visual comparisons of data.

The 3054 DSP System costs $126,950. Delivery is in six weeks.

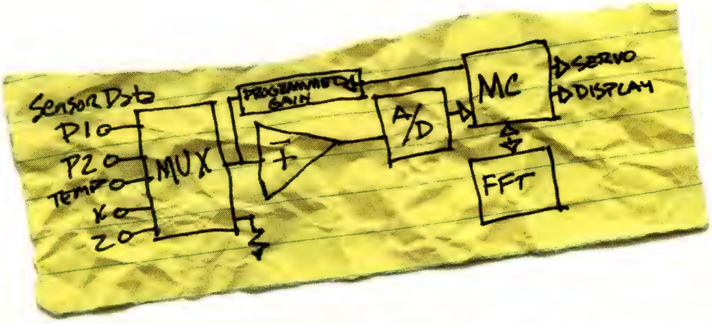
***Tektronix Federal Systems Inc.,** P. O. Box 4495, MS 38-386, Beaverton, OR 97076-4495 (800) 835-9433.* **CIRCLE 613**

■ *JOHN NOVELLINO*

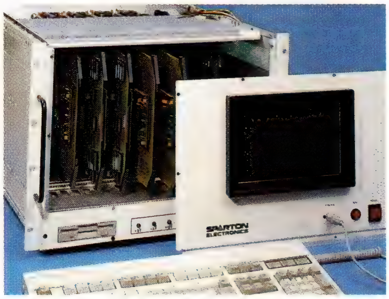
COMTEST BOXES ARE PORTABLE

Three comtest boxes offer portable testing of the RS-232/V.24 interface. The model 52 weighs just 170 g, and measures 103 by 80 by 20 mm. It has 26 red and green monitors and full breakout functionality. The model 100 Compact has 51 monitors and a 30-cm detachable cable. The model 100 Plus can test parallel interfaces and wall-mounted cables. The monitors are line powered and show signal strength. All three testers show full interface activity; all come with jumper cables, a user manual, and a transporting pouch.

Comcraft, 1 Rue des Seigneurs, 67202 Wolfisheim, France; 88 76 50 40.
CIRCLE 614



If You Can Think It,



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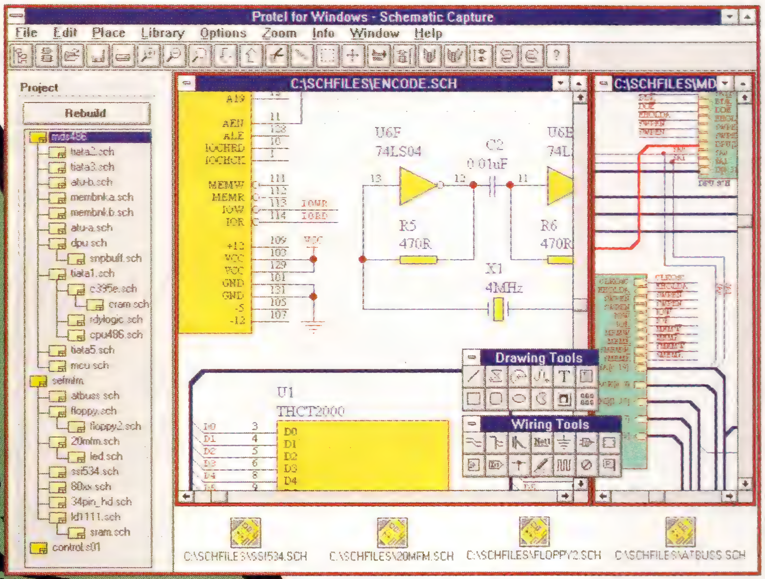
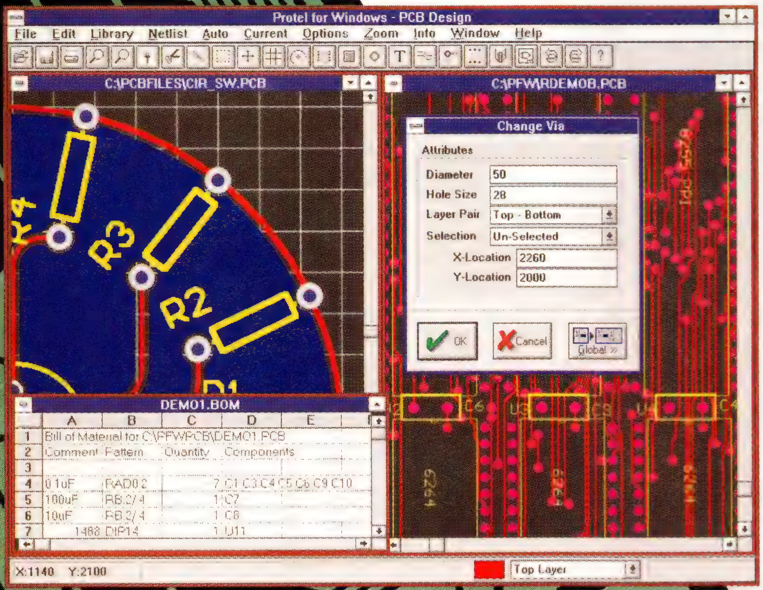


▲ *Advanced Schematic* features dynamic links to the #1 Windows PCB layout system, *Advanced PCB* ▼


Protel for Windows - PCB Design
File Edit Library Netlist Auto Current Options Zoom Info Window Help
C:\PCBFILES\CIR_SW.PCB
C:\PFW\RDEMOB.PCB
R4
R3
R2
D1
X:1140 Y:2100
Top Layer

Change Via

Attributes

Diameter 50
Hole Size 28
Layer Pair Top - Bottom
Selection Un-Selected
X-Location 2260
Y-Location 2000

✓ OK ✗ Cancel Global »

DEM01.BOM

	A	B	C	D	E
1	Bill of Material for C:\PFWPCB\DEM01.PCB				
2	Comment	Pattern	Quantity	Components	
3					
4	0.1uF	RAD0.2	7	C1 C3 C4 C5 C6 C9 C10	
5	100uF	RB.2/.4	1	C7	
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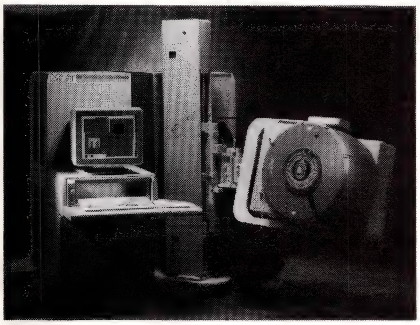
CIRCLE 172 FOR U.S. RESPONSE

CIRCLE 173 FOR RESPONSE OUTSIDE THE U.S.

SYSTEM SCAN TESTS 960-PIN ICs



The advantages that IEEE-1149.1 boundary-scan testing brought to board production test are now available to IC manufacturers using the MCT 1149 Boundary Scan VLSI/ASIC Test System. The tester performs all functional device tests on all boundary-scan and internal-scan devices with up to 960 pins, including FPGAs, gate arrays, standard cell devices, ASICs, MCMs, and 1149.1-compliant standard logic.

Each channel is backed by a memory of up to 128 million vectors, which can be supplied to the device under test at a 50-MHz pattern rate. The ac parametric measurement unit has a measurement accuracy of ±150 ps and a less than 1-ps resolution. Full four-quadrant dc parametric measurement units are available in per-pin or 1-per-8-pin configurations.

The MCT 1149's software toolset allows full porting of simulation vectors from most CAD/CAE systems and complete back annotation to most design systems. The package, which includes an object-oriented, graphics-based vector editor, permits transparent serial-to-parallel vector translation. The system can use 1149.1-compliant boundary-scan description language files.

An innovative I_{DDQ} testing technique used by the MCT 1149 eliminates the need for I_{DDQ} information to undergo a complicated digital-to-analog conversion. As a result, the tester can do I_{DDQ} tests 50 to 100 times faster than other systems, allowing continual I_{DDQ} fault monitoring at functional test rates.

A 512-pin MCT 1149 with basic dc measurement capability costs about $500,000. A high-end version with added dc capability and ac measurement functions costs about $850,000. Estimated delivery time is 120 days.

Micro Component Technology Inc.*, 2635 N. First St., Suite 101, San Jose, CA 95134; (408) 432-3200.*

CIRCLE 615

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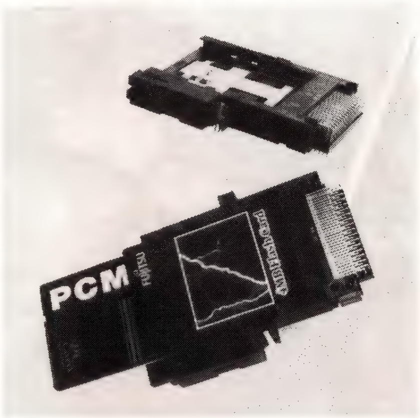
CIRCLE 216 FOR U.S. RESPONSE
CIRCLE 217 FOR RESPONSE OUTSIDE THE U.S.

PCMCIA CONNECTORS STACK TO SAVE SPACE



Two memory-card slots take about the same space as one when using the FCN565 Series stacked memory-card connectors. The connectors, which accept both Types I and II memory cards and meet all JEIDA and PCMCIA specifications, consist of two stacked, 68-position, right-angle headers. They're available with or without ejection mechanisms to aid in card removal. Contact pitch is 0.050 by 0.050 in. for each slot. Terminals are configured in an eight-row zig-zag pattern with 0.075-in. spacing between rows. Pricing with an ejection mechanism is $11.04 in lots of 1000. Samples are available now.

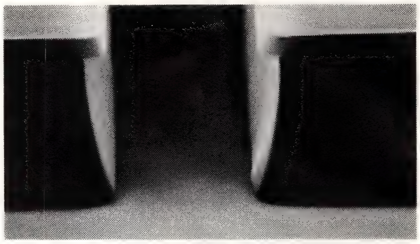
Fujitsu Microelectronics Inc., Electronic Components Div., 3545 N. First St., San Jose, CA 95134; (800) 642-7616. **CIRCLE 617**

HIGH-DENSITY CONTACTS CONTROL IMPEDANCES

A 50-Ω micro-coaxial contact designed for high-speed data transfers is the linchpin of the har-pak 2.5-mm connector system. The connector modules feature 2, 4, or 6 contacts in 25 mm of board edge and come in solder or press-in versions. They're compatible with 19-in. rack equipment. Their high density permit up to 60 coaxial connections on a double-high Eurocard. The low-insertion-force contacts are rated for frequencies up to 2 GHz and a VSWR of 1.25:1. Insertion loss is 0.25 dB. The connectors are available now. Call for pricing.

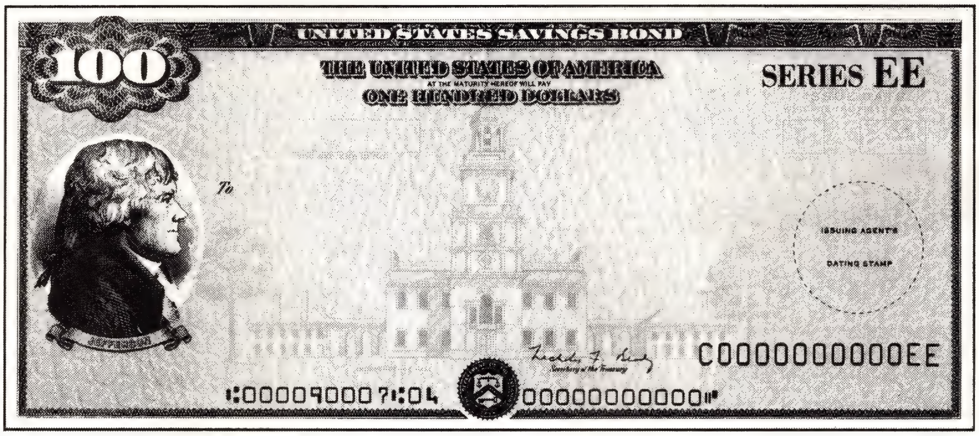
Harting Elektronik Inc., 2155 Stonington Ave., Hoffmann Estates, IL 60195; (708) 519-7700. **CIRCLE 618**

SUBSTRATE COATINGS LOWER MCM COSTS



Cost will greatly influence the viability of multichip-module (MCM) packaging technology. The 4000 Series of Ultradel microelectronic coatings are a cost-effective solution for high-density MCM-D (deposited thin-film) substrates. The inherent properties of the polymide material, such as ease of processing, low dielectric constant, superior planarization, and high temperature stability, make the Ultradel 4000 coatings desirable. The coatings are easily patterned using Amoco's wet-patterning method—a low-cost alternative to conventional dry etching. Call for pricing.

Amoco Chemical Co., 200 E. Randolph Dr., Chicago, IL 60601-7125; (312) 856-3200. **CIRCLE 619**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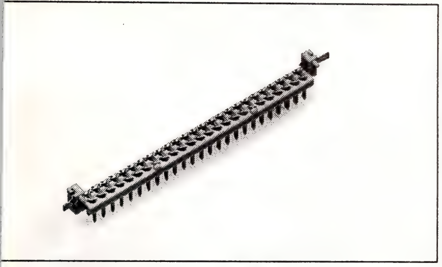

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ectors ideal for HHD applications.
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eader. FAP features 2 in 1 design with
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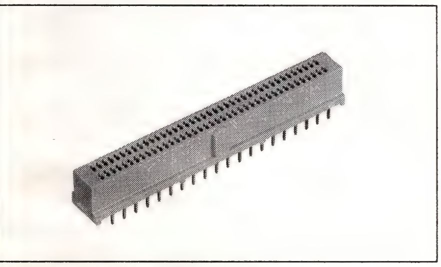

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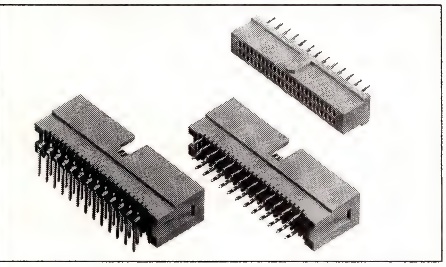

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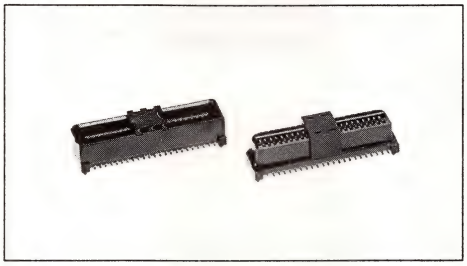
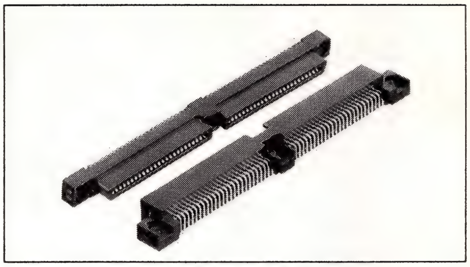
Circle 279





Circle 280

NDS/NDP Series SMT type 1.27mm pitch board-to-board connectors. Low profile mating design with blade-to-blade type contacts. Available in 36 to 128 leads Right Angle or Straight.

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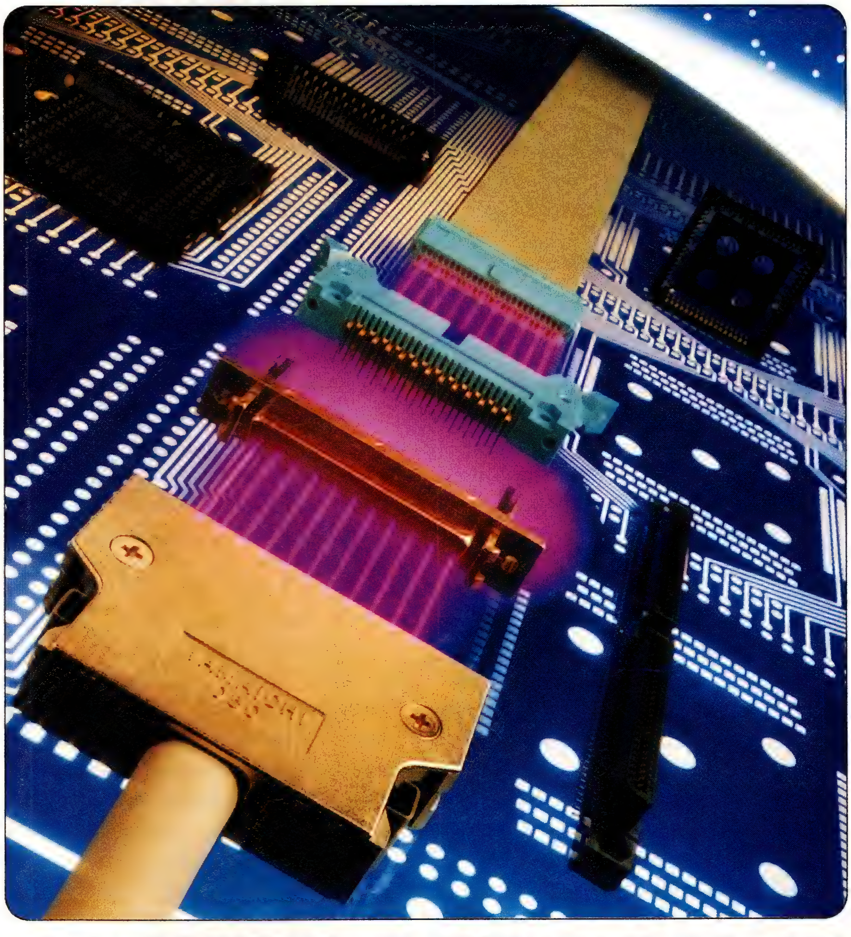

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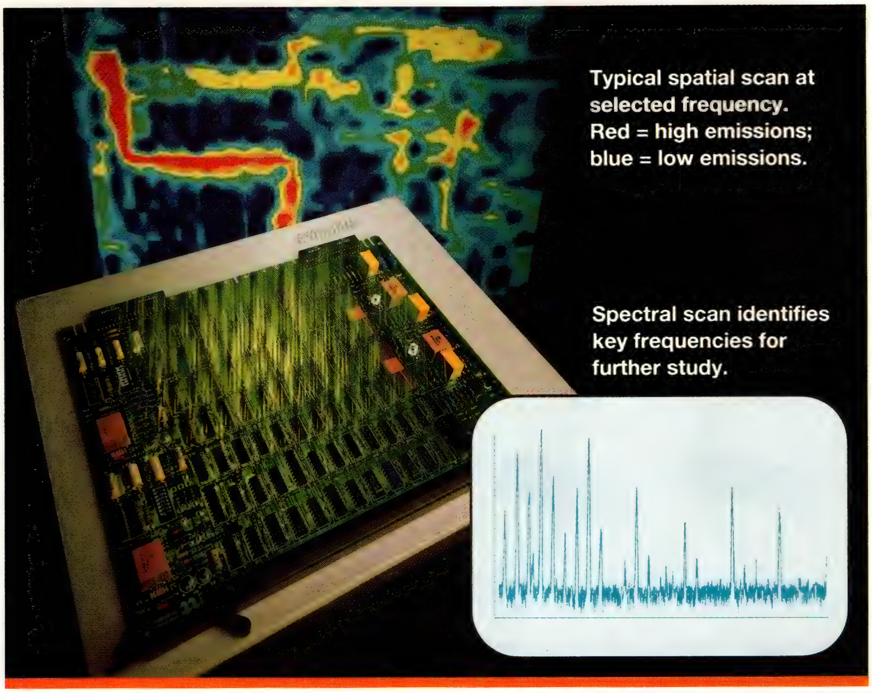
CIRCLE 281 FOR U.S. RESPONSE CIRCLE 282 FOR RESPONSE OUTSIDE THE U.S.


Typical spatial scan at selected frequency. Red = high emissions; blue = low emissions.
Spectral scan identifies key frequencies for further study.

Catch emissions problems at board level, where compliance fixes are least costly.

Now you can quickly get a color image of the electromagnetic performance of your printed-circuit board or subassembly *before* final compliance testing. Spatial and spectral displays generated by the EMSCAN PCB emissions scanner show you which frequencies and which areas of the board under test are guilty. These scans are stored for later comparison after design alterations, to check whether offending emissions are now down to acceptable levels.

Just plug your receiver or spectrum analyzer, and your computer with IEEE-488 interface, into the EMSCAN scanner, and a matrix of 1280 H-field probes maps the area of your test board (up to 9" x 12") for high, medium, and low-emissions spots within the 10-to-750-MHz frequency range. Or you can see a spectral display showing the overall condition of the board across the spectrum. You may then choose a frequency of particular interest for intensive spatial examination.

After the development stage, you can use EMSCAN as a quality-control tool, checking completed boards against a "good" scan before they go into assembly. This is the point where production compliance becomes virtually assured.

The software operates under "Windows" to make early diagnosis easy, even for those who are new to compliance testing. It can run on several PCs and workstations, and is readily ported to other environments for analysis.

You should learn all about this qualitative and quantitative measure of emissions for use during product development—where design corrections are least costly. To start, call toll-free (1-800-933-8181) to speak with an applications engineer and arrange to see a demonstration in your office or plant.

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CIRCLE 86

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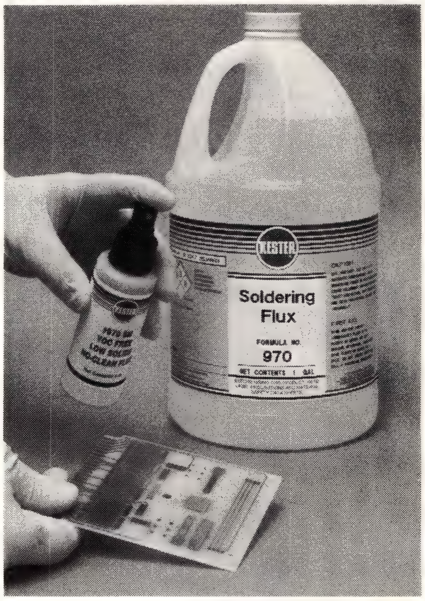

A no-clean flux that's free of volatile organic compounds (VOCs) claims to be the first of its kind. The Kester 970 flux offers greater productivity and reliability for board assemblies. Because the flux is both VOC- and CFC-free, and meets increasingly stringent U. S. Government regulations for chemical-waste disposal, it cuts manufacturing costs by eliminating the need for hazardous-chemical removal and disposal. More cost savings are garnered by elimination of cleaning costs. Call for pricing and delivery.

Kester Solder, 515 E. Touhy Ave., Des Plaines, IL 60018; (708) 297-1600. **CIRCLE 620**

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A combination of a forced-convection heat sink and fan that sits directly on top of a CPU dissipate the IC's heat, eliminating the problems associated with overheating. The Icecap-4 thermal-management product alleviates loss of data, generation of errors, and computer shutdown. It extends the life of costly semiconductors and is designed for use on any microprocessor, gate array, or floating-point coprocessor. The device is optimized for circuits dissipating between 1 and 35 W and maintains IC-case temperatures at or below manufacturer's recommended maximum temperatures. It measures 1.6 by 1.6 by 0.6 in. and weighs 1.3 ozs. Pricing is $18 for lots of 100. Small quantities are delivered from stock.

ICECAP Technologies, 3080 Oakmead Village Dr., Santa Clara, CA 95051; (408) 727-6100. **CIRCLE 621**

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CIRCLE 186 FOR U.S. RESPONSE CIRCLE 187 FOR RESPONSE OUTSIDE THE U.S.

CMOS 8-BIT CURRENT-OUTPUT DAC RUNS OFF 3.3-V SUPPLY RAIL

Offering pin and function compatibility with the standard multiplying d-a converter, the CMOS ALD1801, a bipolar DAC-08 from Advanced Linear Devices, consumes 3% of a DAC-08's supply current—just 500 μA maximum from a single 3.3-V supply rail; 800 μA from a 5-V rail. That represents power dissipations of just 1.8 mW and 4.5 mW, respectively. Fully specified for 3.3-V/±1.65-V and 5/±2.5-V operation, it handles 12 V between the supply pins.

Special versions can be provided for operation from ±1-V rails. Full-scale output current runs 100 μA and 50 μA from 5- and 3.3-V rails respectively. Compliance voltage is 2.5 V minimum with 5-V supplies, a volt less with 3.3-V supplies. All grades are 8-bit monotonic and maximum non-linearity runs ±0.1, ±0.19, and ±0.39% for the 1801A, 1801B, and 1801, respectively. The reference-input amplifier is unity-gain stable so, unlike the DAC-08, off-chip compensation capacitors are not required. Settling times to 1/2 LSB for a full scale step runs 5 μs off 5-V rails, twice that off 3.3-V rails. Available in 8-pin plastic and ceramic DIPs, as well as SOICs, pricing in quantities of 100 starts at $2.09 each in plastic DIPs.

***Advanced Linear Devices,** 1180F, Miraloma Way, Sunnyvale, CA 94086-4606; (408) 720-8737* **CIRCLE 622**

■ *FRANK GOODENOUGH*

VIDEO SWITCH CUTS ON-RESISTANCE

On resistance of CMOS analog switches typically run significantly more than 10 Ω. But the Silconix dual DG642 and quad DG641 provide typical on resistances of 5 Ω and 8 Ω, respectively, with a switch current of 10 mA. Maximum on-resistance over temperature still lies under 9 Ω and 20 Ω, respectively. Designed for true relay replacement in professional A/V equipment and precision test instruments, they can switch dc, analog, and digital signals. At 5 MHz, both provide maximum all-hostile crosstalk of –85 dB between channels and its typically still –40 dB at 100 MHz.

In a 75-Ω circuit, off isolation at 5 MHz runs –60 dB maximum. When on, the switches' 3-dB bandwidth in a 50-Ω circuit typically runs 500 MHz. Turn-on/off time for the DG641, when driving 1000 Ω in parallel with 35 pF, runs a maximum of 70 ns and 50 ns, respectively. Both switches handle currents to 75 mA, which lends them well to switching current sources in ATE applications and driving capacitive loads. Low rc time constant adapts them for rf switching applications. In quantities of 1000, in a 16-pin DIP, the DG641 goes for $1.80 each; $1.96 each in an SO-16. In similar quantities, the DG642 goes for $1.74 each in an 8-pin DIP; $1.83 in an SO-8.

***Siliconix Inc.,** 2201 Laurelwood Rd., Santa Clara, CA 95054; (800) 554-5565, ext. 81.* **CIRCLE 623**

■ *FRANK GOODENOUGH*

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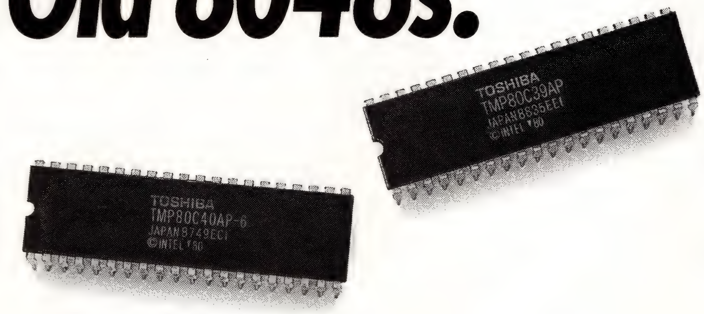

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CIRCLE 248 FOR U.S. RESPONSE
CIRCLE 249 FOR RESPONSE OUTSIDE THE U.S.

"Without advertising, everybody would think Ronald was just the name of a former president."

Mike Quinlan, Chairman, CEO McDonald's (left)

"The remarkable thing is, when you think about McDonald's® you've got to think about people. A friendly crew person welcoming you. Kids, moms and dads having a good time at McDonald's, even a funny clown named Ronald.® Those pictures in your mind are advertising at work.

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CIRCLE 236 FOR U.S. RESPONSE

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IC LINKS SENSORS, CPUS

Called the Prosensor, the SSC 8830 from Telephonics operates between low-level sensors and microprocessors performing both signal conditioning and a-d conversion. This unique, 10-bit accurate device is aimed at low-cost data acquisition of data directly from accelerometers, strain gages, and pressure transducers. Applications range from air conditioning and process control to weigh scales and automotive.

It takes a differential or single-ended low-level (as small as 3 mV full scale) dc input from a sensor and multiplies (or chops) it by a sampling frequency. The chopped signal is converted back to a dc voltage level and fed to a delta-sigma modulator. The pulse train from the ADC is fed to a host processor or microcontroller. It latches the pulse stream, with the sampling clock driving the chopper, and returns the stream to the Prosensor. A low-pass filter built with an on-chip resistor and off-chip capacitor integrates the pulse stream, converting it to a voltage. The SSC 8830 then compares this voltage to the amplified input signal closing a loop. The processor measures input voltages by counting the number of logic one pulses over a fixed period of time, essentially decimating the pulse train.

In quantities of 2500, the SSC 8830 goes for $2.40 each in its 16-pin DIP or SOIC.

***Telephonics Corp.**, 815 Broad Hollow Rd., Farmingdale, NY 11735; (516) 755-7046.* **CIRCLE 624**

■ *FRANK GOODENOUGH*

IC INSTRUMENTATION AMPS GET SPEED

To fill performance inexpensively, Burr-Brown has three new instrumentation amplifiers. The fastest one, the INA111 has JFET inputs; the INA115 offers increased precision; and the INA131 has a precise, fixed gain of 100. The INA131 shares its gain between input and output stages to increase common-mode voltage range; the INA111 incorporates current-feedback techniques to maximize bandwidth.

The INA111's use of current feedback op amps gives it a typical 2-MHz 3-dB bandwidth to gains beyond 10, 450 kHz at a gain of 100, and bandwidth of 50 kHz at a gain of 1000. With voltage feedback, 3-dB bandwidths at the same gains would drop from 2 MHz to 2 kHz. The INA115's strength is its architecture and precision. The design permits driving shields and/or the use of an external IC multiplexer to turn it into a PGA. Its maximum offset voltage runs less than 50 μV, while CMRR runs better than 115 dB at a gain of 1000; better than 80 dB at a gain of 1. The INA131 provides similar performance, but on chip laser-trimmed resistors provide a guaranteed fixed gain of 100 ±0.024%. Gain temperature coefficient runs a maximum of ±10 ppm/°C from –40°C to +85°C. The unit price in 1000's starts at $3.25 for the INA111 and INA131, and $3.65 for the INA115.

***Burr-Brown Corp.**, P.O. Box 11400, Tucson, AZ 85734; (800) 548-6132* **CIRCLE 625**

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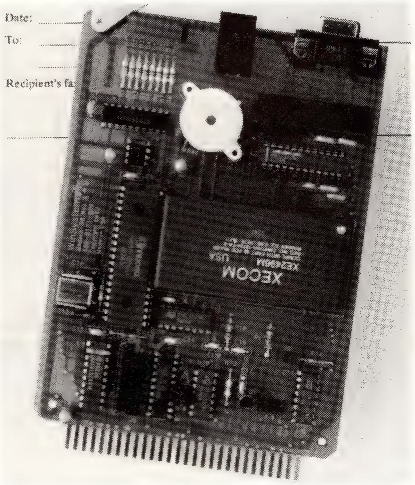
CIRCLE 196 FOR U.S. RESPONSE CIRCLE 197 FOR RESPONSE OUTSIDE THE U.S.

FAX-MODEMS FIT STD BUS



Targeted at industrial, embedded applications, three integrated boards put fax-modem capabilities onto the STD bus. The boards implement the industry-standard Class 1 AT fax and data command set to communicate with other PCs or fax machines, even in remote or unattended applications.

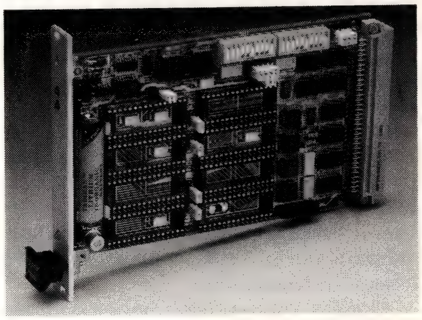
The MCM-2496 is a 9600-bit/s send-only fax card. The 9624 and 9696 send and receive at 9600 bits/s. The 2496 and 9624 send and receive modem data at 2400 bits/s, while the 9696 works at 9600 bits/s. All three boards are compatible with Bell and International CCITT data-communication standards. In addition, they support Group III 9600-bit/s fax with fall-back speeds of 4800 and 2400 bits/s. For modem use, MNP levels 2 through 5 are supported for error correction and detection.

Using a serial interface, the boards can be connected to RS-232 serial ports from other boards with either a 9- or a 25-pin connector. A speaker and eight LEDs supply the modem's handshake and data-line status. They also display transmit and receive data, request and clear to send, ring indicator, data-carrier detect, and off hook. Available now, the 2496 sells for $399; the 9624 for $495; and the 9696 for $895.

***WinSystems**, 715 Stadium Dr., Suite 100, Arlington, TX 76011; (817) 274-7553.* **CIRCLE 626**

■ *RICHARD NASS*

RAM/ROM/FLASH FIT 3U VME FORM FACTOR



The XVME-103 RAM/ROM/flash memory module for VMEbus systems holds up to 8 Mbytes of EPROM or 4 Mbytes of CMOS/flash. The single-height (3U) module organizes the memory into two independently addressable banks of four 32-pin sockets. Power-down memory protection insures data integrity when using CMOS devices. CMOS memory can be backed up by an on-board battery. Without memory devices, prices start at $450.

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CIRCLE 156 FOR U.S. RESPONSE
CIRCLE 157 FOR RESPONSE OUTSIDE THE U.S.

SIMULATION DATA MANAGEMENT

SOURCE III provides a suite of CAE tools for dealing with the generation, translation, verification and analysis of logic simulation data files. The software is available on most workstation platforms and interfaces to over 25 popular logic simulators.

VGEN® — VECTOR GENERATION
VGEN is a high-level, simulator-independent Stimulus Generation language that makes it easy to create, modify, document and maintain simulation stimulus files. **VGEN** can reduce stimulus development time by up to 80% and provides a common front-end to most logic simulators.

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VTRAN is a vector translator which provides a vital link between the many dissimilar logic simulation data formats in use today. **VTRAN** solves the data translation problems inherent in applying multiple simulation and verification tools to a design project. **VTEST** works with **VTRAN** to create functional test programs for device testers from simulation results data.

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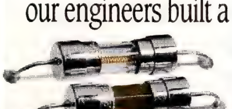

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MIL-SPEC 6U VME BOARD SUPPORTS PARALLEL-PROCESSING APPLICATIONS

The 6U MZ 7775 multiprocessor digital-signal processor for the VMEbus fully conforms to military specifications. The board is built with four TI SMJ320C40 DSP chips, each capable of 40 MFLOPS. Consequently, the board was built for parallel-processing applications.

The board comes with 512 kbytes or 1 or 2 Mbytes of 32-bit-wide global memory, which can be accessed by all four of the DSP chips. Each processor is connected to six 16-Mbyte/s communication channels for high-speed interprocessor communication. In addition, each chip has its own local memory, made up of 32-bit static RAM. Memory configurations range from 2.5 to 10 Mbytes. Flash EPROM is available for startup or boot code.

The board's I/O, which is available through the P2 connector on the VMEbus backplane, is completely programmable and includes VSB as an option. Applications include guidance systems and command and control systems.

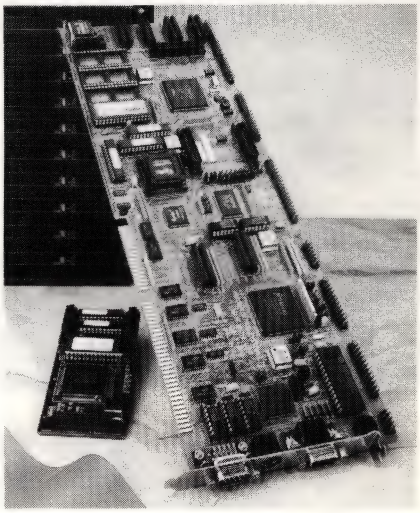
The MZ 7775 comes with a series of software support tools, including an ANSI-compatible C compiler with a parallel run-time library, a C source-level debugger, TI's pDSP XDS 510 in-circuit emulator with JTAG diagnostic support, and an Ada compiler. Available now, the MZ 7775 sells for $34,500 with 5 Mbytes of SRAM and 1 Mbyte of EPROM.

Mizar Inc., 2410 Luna Rd., Carrollton, TX 75006; (214) 247-8849.

CIRCLE 628

■ RICHARD NASS

486SLC BOARD FOR EMBEDDED APPLICATIONS



Designed around the 486SLC CPU, the PSCIM486SLC AT-compatible processor board can handle industrial or embedded applications. The board integrates all the functionality of a PC/AT motherboard on one full-length card. This approach allows a 486-based PC to be built on a passive backplane. In addition to holding 768 kbytes of flash EPROM and a Super VGA controller, it can handle 8 Mbytes of DRAM and 128 kbytes of battery-backed SRAM. Utilities for implementing DOS applications in a silicon disk are available.

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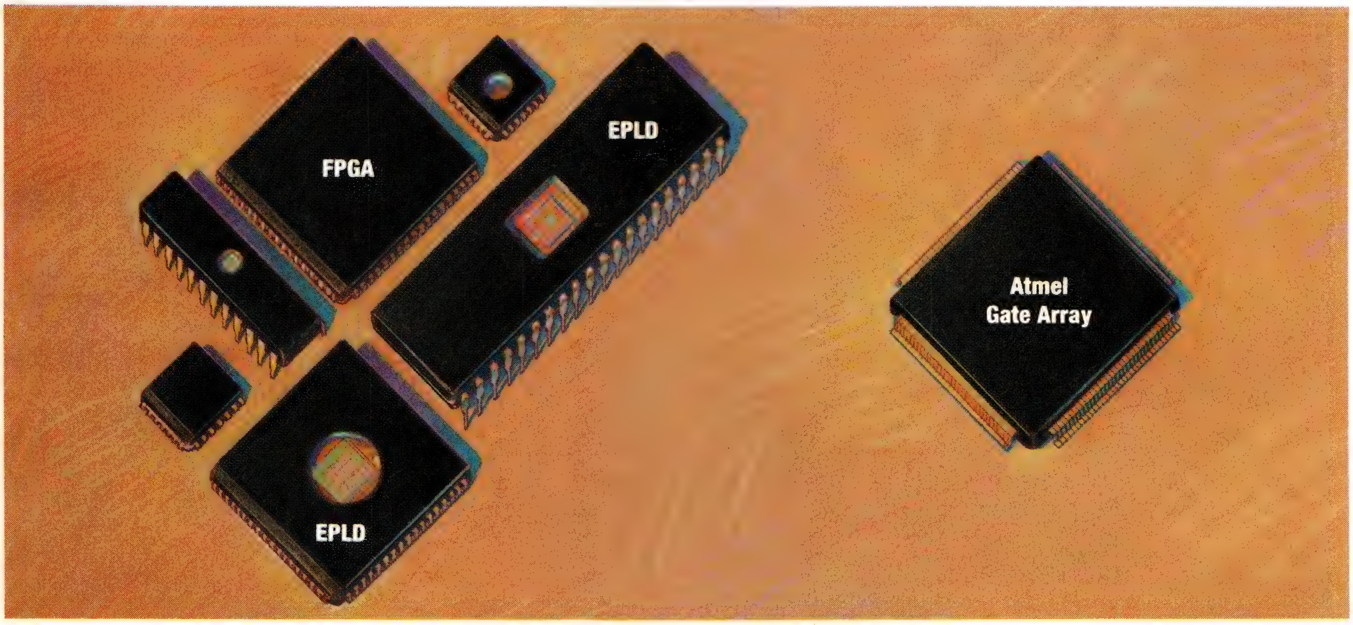

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Powercube Corp., 8 Suburban Park Dr., Billerica, MA 01821; Roy Allman, (508) 667-9500. **CIRCLE 630**

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International Rectifier Inc., 233 Kansas St., El Segundo, CA 90245; (310) 607-8978. **CIRCLE 631**

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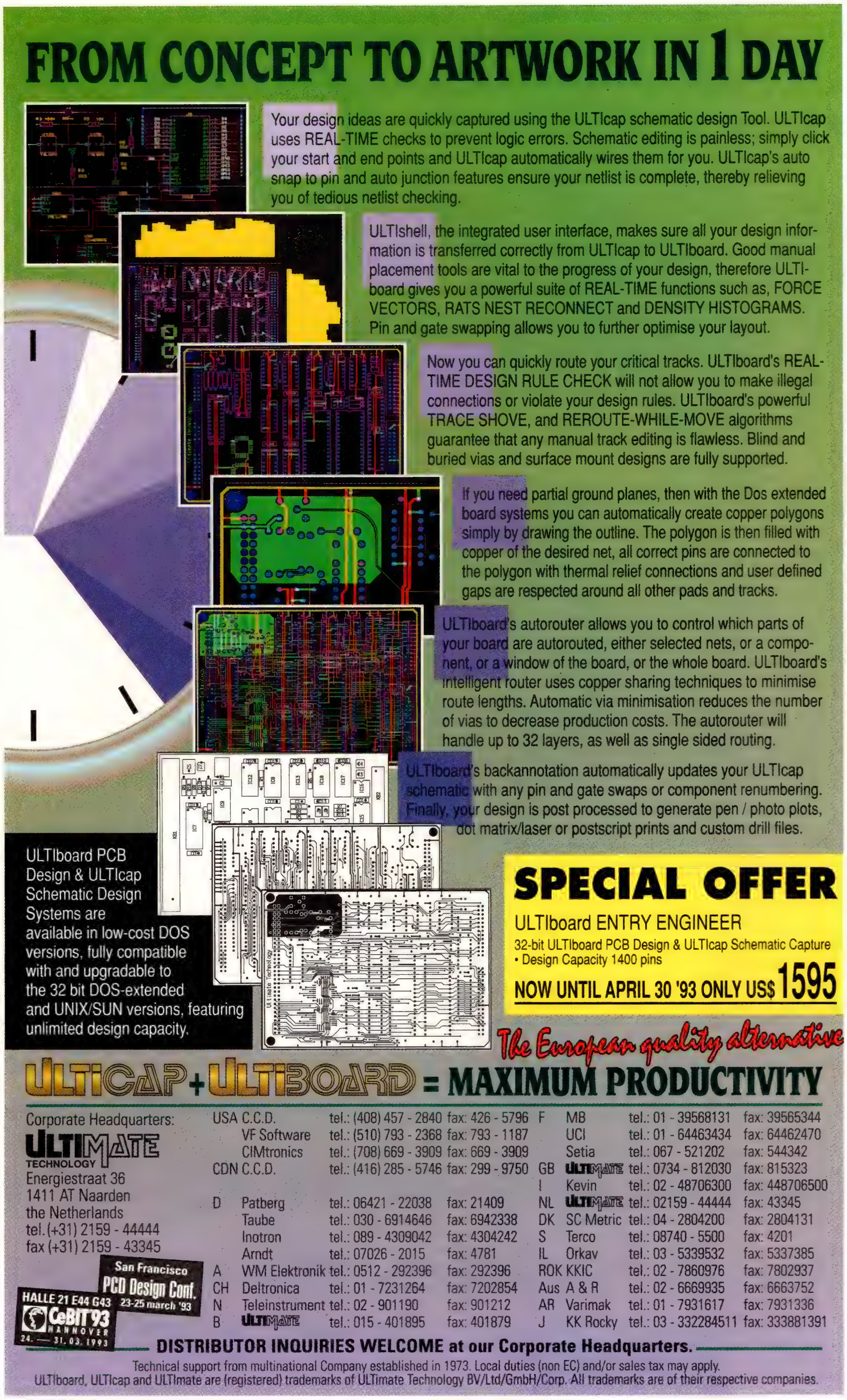
Advanced Power Technology, 405 S.W. Columbia St., Bend, OR 97702; (503) 382-8028. **CIRCLE 632**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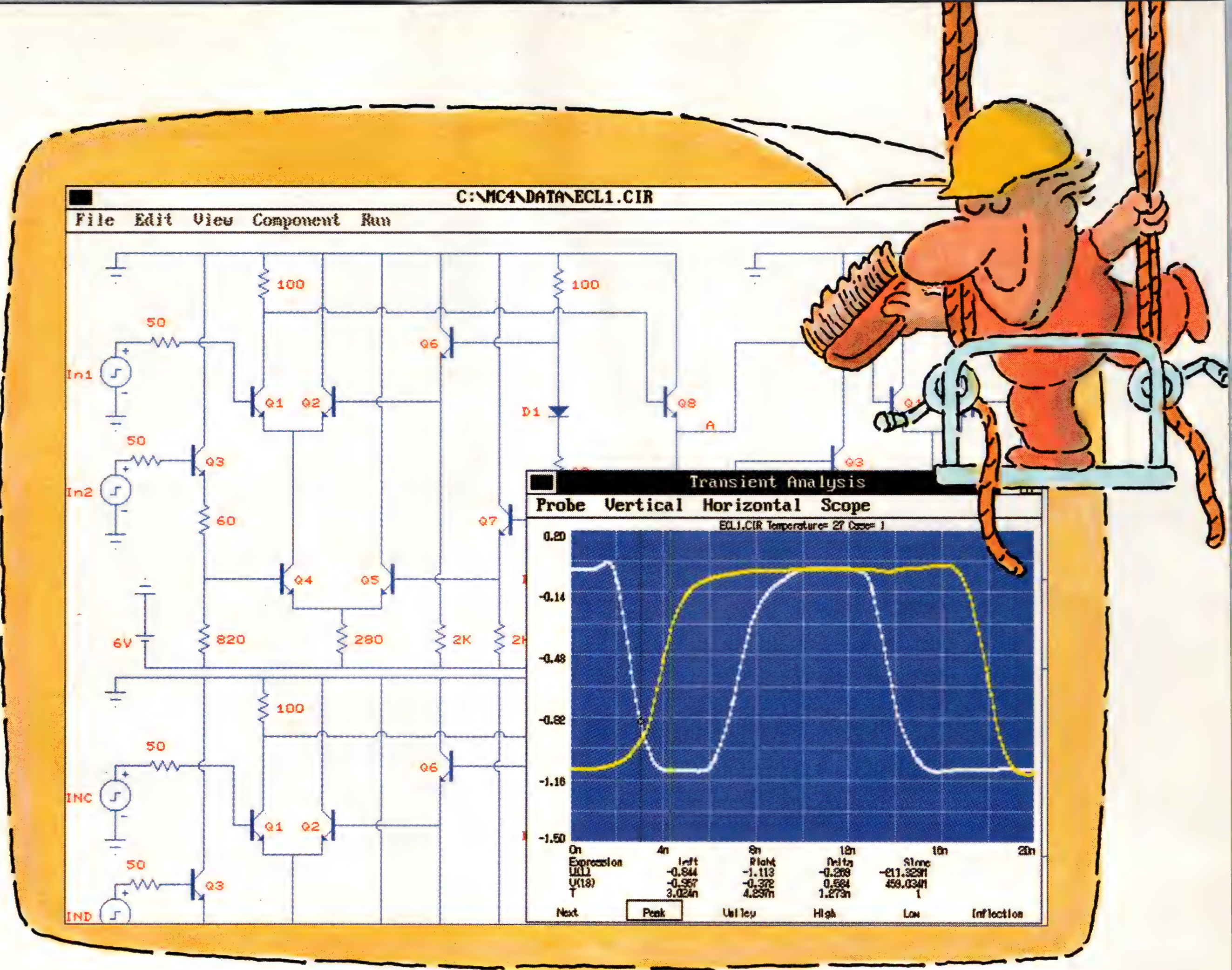

```
Expression      Left      Right     Delta     Slope
V(1)          -0.844     -1.113    -0.269  -211.329M
V(18)         -0.957     -0.372     0.584   459.034M
T              3.024n     4.297n    1.273n         1
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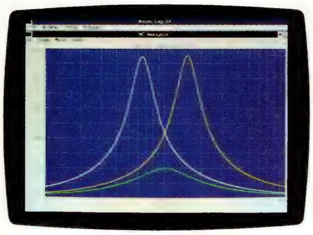

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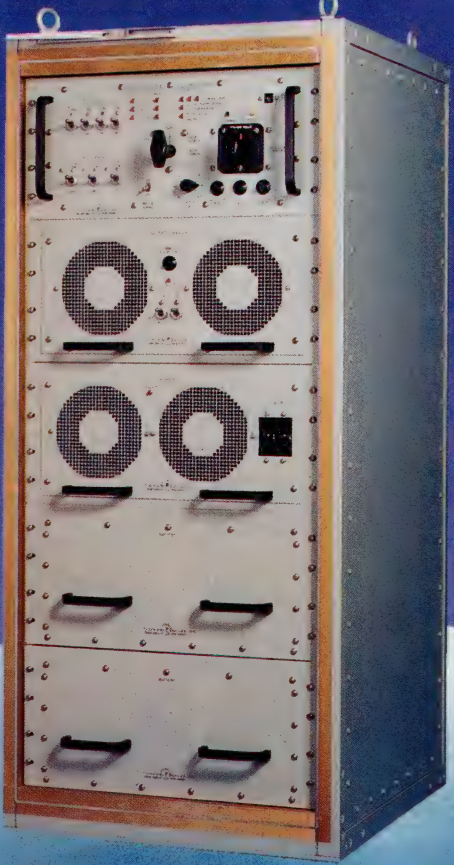

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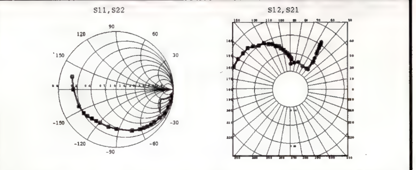

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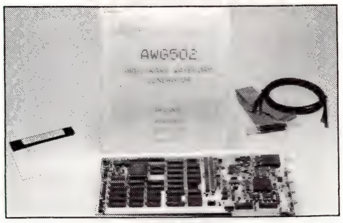

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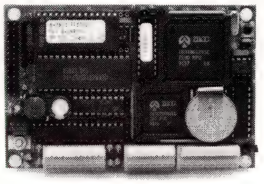

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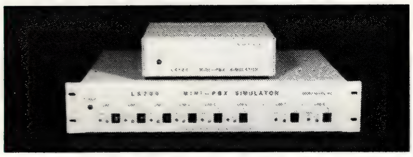

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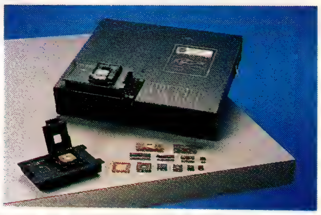

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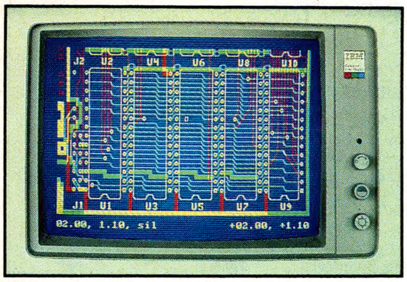

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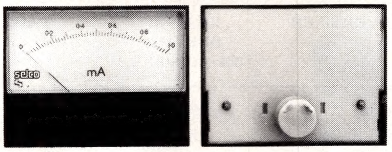

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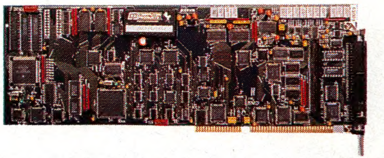

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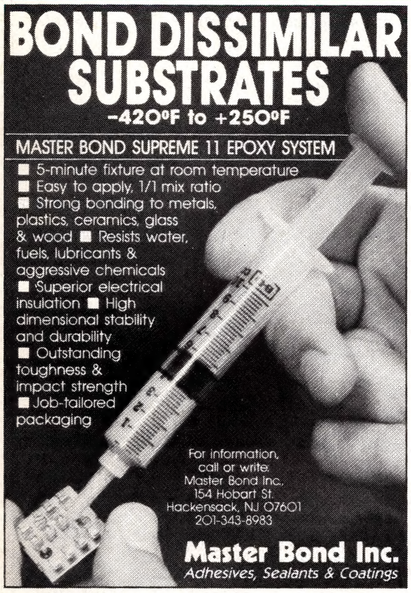

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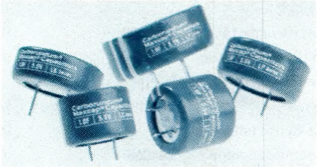

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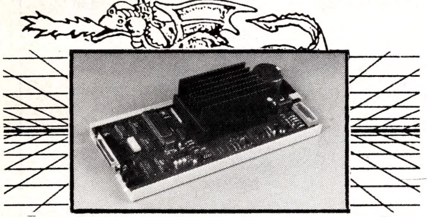

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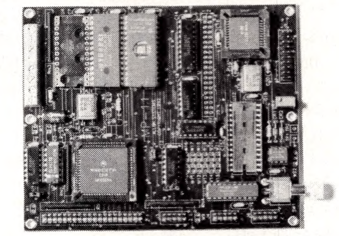

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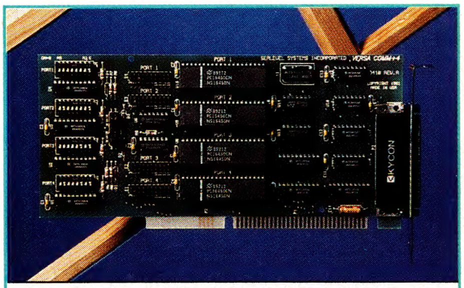

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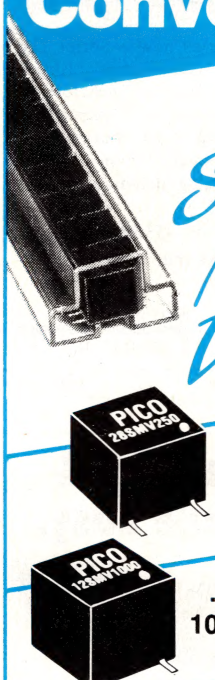

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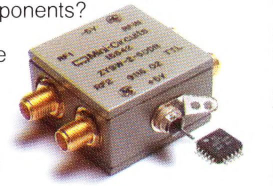

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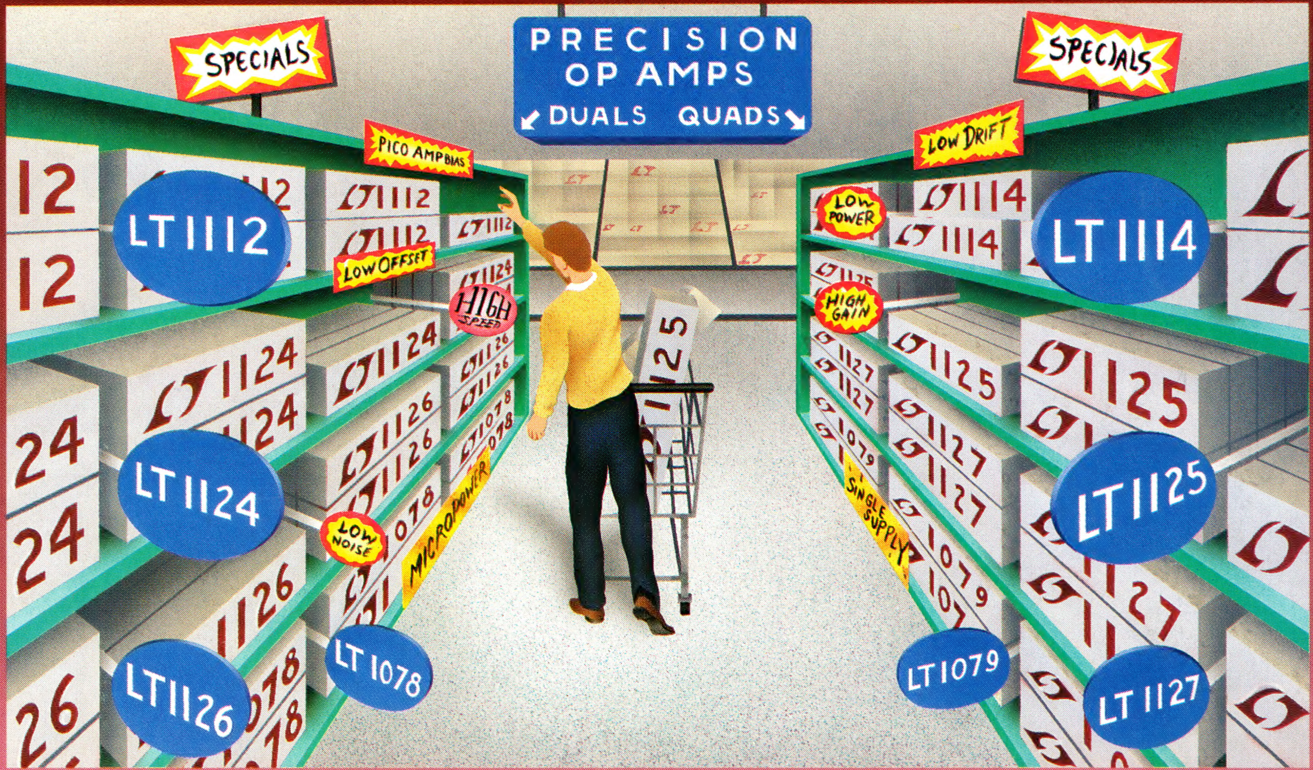

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